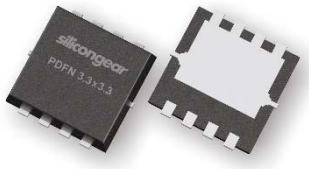
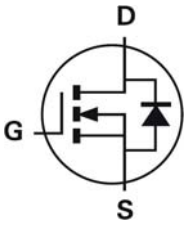
DG100N14E

DG-FET™ 100V N-Channel Power MOSFET

Key Performance Parameters		
Parameter	**Value**	**Unit**
V_{DSS}	100	V
$R_{DS(ON)\ max.}$ V_{GS}=10V	15	mΩ
$R_{DS(ON)\ max.}$ V_{GS}=4.5V	22	mΩ
I_D	37	A
Q_g	21.23	nC
Q_{gd}	5.65	nC

PDFN 3.3x3.3-8L





Features	Application
• Optimized for synchronous rectification Low Input Capacitance • Low Miller Capacitance • Fully Characterized Capacitance and Avalanche • Pb-free lead plating; RoHS compliant	• BLDC Motor drive applications • Battery powered circuits • Synchronous rectifier applications • Resonant mode power supplies

Ordering Information

Ordering Code	RoHS Status	Package	Package Code	Packing	Quantity
DG100N14E	Halogen-Free	PDFN 3.3x3.3-8L	E	Tape & Reel	5,000

Absolute Maximum Ratings (T_J=25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous	T_C=25°C	I_D	37	A
	T_C=100°C		24	A
Drain Current-Pulsed Note 1	T_C=25°C	I_{DM}	60	A
Avalanche Current		I_{AS}	15	A
Single Pulse Avalanche Energy Note 3		E_{AS}	11	mJ
Maximum Power Dissipation	T_C=25°C	P_{tot}	35.7	W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Thermal Resistance Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Ambient Note 2	$R_{\theta JA}$	Steady State	-	-	60	°C/W
Thermal resistance, Junction-to-Case	$R_{\theta JC}$	Steady State	-	-	3.5	°C/W

Notes:

1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
2. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 in still air.
3. Limited by T_{Jmax}, starting T_J=25°C, L=0.1mH, R_g=50Ω, I_D=15A, V_{GS}=10V.

Electrical Characteristics (T_J=25°C unless otherwise noted)

STATIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_{DS}=10mA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V, T_J=25°C	-	-	10	µA
		V_{DS}=100V, V_{GS}=0V, T_J=125°C	-	-	100	µA
Gate-Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA

STATIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_{DS}=250µA	1.2	1.7	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_{DS}=12A	-	-	15	mΩ
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_{DS}=7A	-	-	22	mΩ
Gate Resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz	-	0.5	-	Ω
Forward Transconductance	g_{fs}	V_{DS}=5V, I_{DS}=12A	-	20	-	S

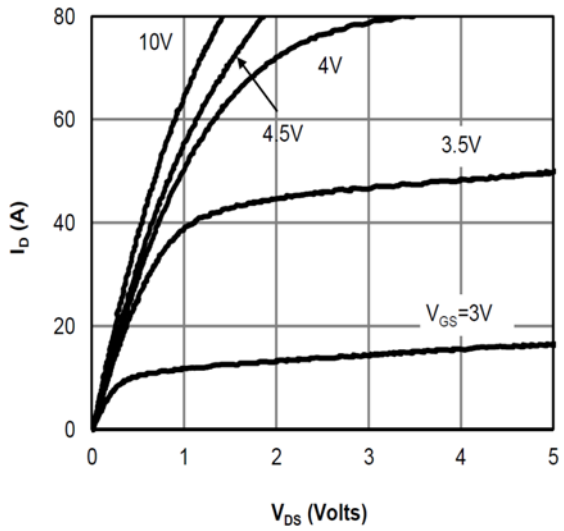
DYNAMIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Input Capacitance	C_{iss}	V_{DS}=50V, V_{GS}=0V, f=1MHz	-	955	-	pF
Output Capacitance	C_{oss}	V_{DS}=50V, V_{GS}=0V, f=1MHz	-	172	-	pF
Reverse Transfer Capacitance	C_{rss}	V_{DS}=50V, V_{GS}=0V, f=1MHz	-	30	-	pF
Turn-On Delay Time	$T_{d(on)}$	V_{DS}=50V, V_{GS}=10V, I_{DS}=12A, R_{GEN}=3Ω	-	7.2	-	ns
Rise Time	t_r	V_{DS}=50V, V_{GS}=10V, I_{DS}=12A, R_{GEN}=3Ω	-	11.8	-	ns
Turn-Off Delay Time	$T_{d(off)}$	V_{DS}=50V, V_{GS}=10V, I_{DS}=12A, R_{GEN}=3Ω	-	18.4	-	ns
Fall Time	t_f	V_{DS}=50V, V_{GS}=10V, I_{DS}=12A, R_{GEN}=3Ω	-	4.6	-	ns

GATE CHARGE CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Gate to Source Gate Charge	Q_{gs}	V_{DD}=50V, I_D=12A, V_{GS}=0 to 10V	-	4.27	-	nC
Gate charge at threshold	$Q_{g(th)}$	V_{DD}=50V, I_D=12A, V_{GS}=0 to 10V	-	1.93	-	nC
Gate to Drain Charge	Q_{gd}	V_{DD}=50V, I_D=12A, V_{GS}=0 to 10V	-	5.65	-	nC
Switching charge	Q_{SW}	V_{DD}=50V, I_D=12A, V_{GS}=0 to 10V	-	7.99	-	nC
Gate charge total	Q_g	V_{DD}=50V, I_D=12A, V_{GS}=0 to 10V	-	21.23	-	nC
Gate charge total	Q_g	V_{DD}=50V, I_D=12A, V_{GS}=0 to 4.5V	-	11.39	-	nC
Gate plateau voltage	$V_{plateau}$	V_{DD}=50V, I_D=12A, V_{GS}=0 to 10V	-	3.81	-	V
Gate charge total, sync. FET (Q_g- Q_{gd})	$Q_{g(sync)}$	V_{DS}=0.1V, V_{GS}=0 to 10V	-	15.58	-	nC

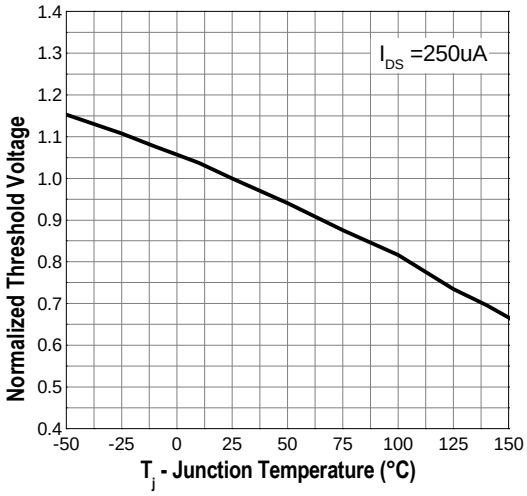
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Diode continuous forward current (Body Diode)	I_S	T_C=25°C	-	-	37	A
Diode pulse current (Body Diode)	I_{SM}	T_C=25°C	-	-	62	A
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=12A	-	0.7	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	V_{DD}=50V, I_F=12A, di/dt=100A/µs	-	49	-	ns
		V_{DD}=50V, I_F=12A, di/dt=200A/µs	-	29	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}	V_{DD}=50V, I_F=12A, di/dt=100A/µs	-	89	-	nC
		V_{DD}=50V, I_F=12A, di/dt=200A/µs	-	69	-	nC

Typical Operating Characteristics

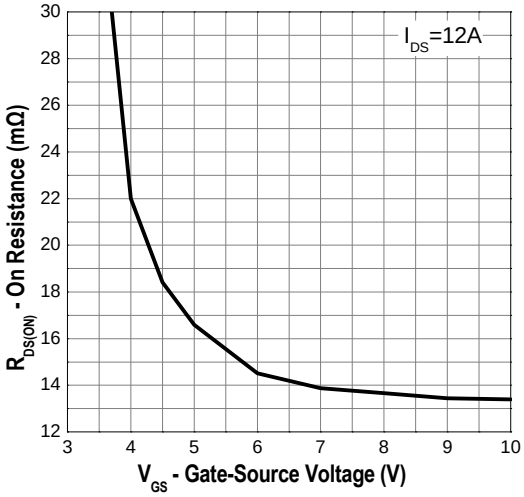
Output Characteristics



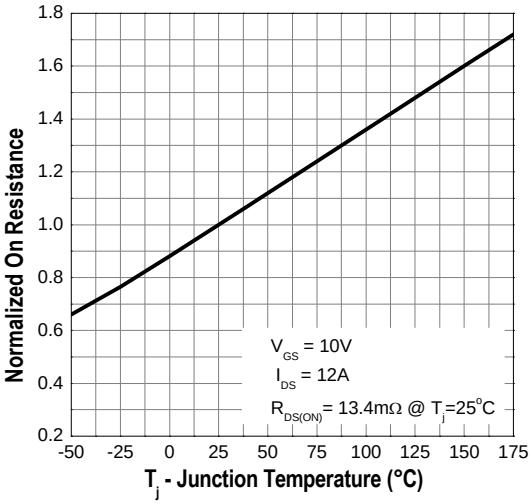
Gate Threshold Voltage



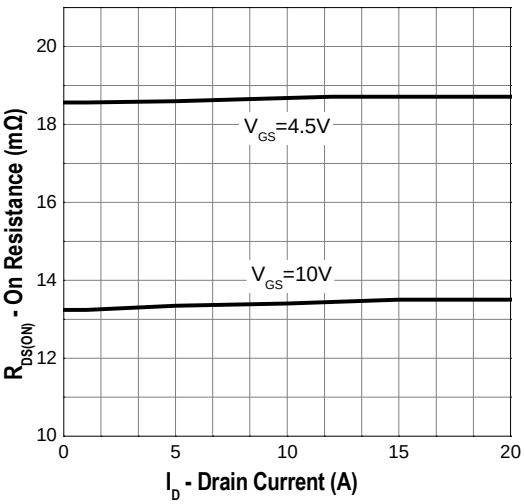
Gate-Source On Resistance



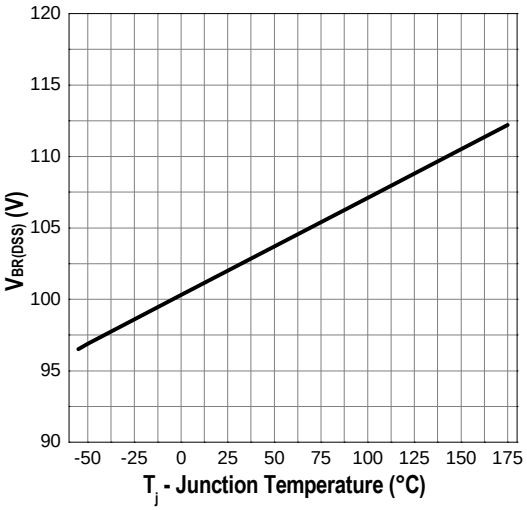
Drain-Source On Resistance



Drain-Source On Resistance

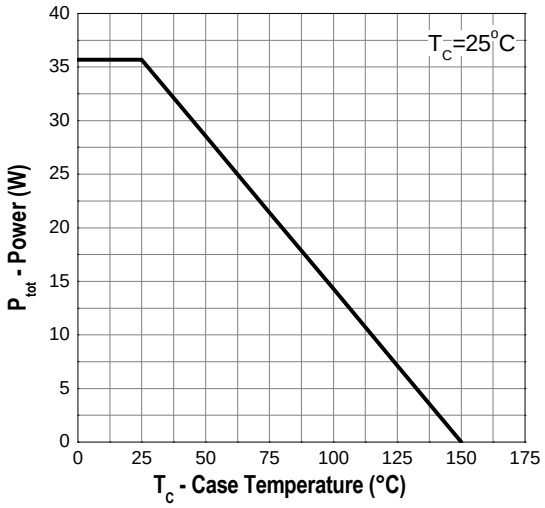


Drain-source Breakdown Voltage

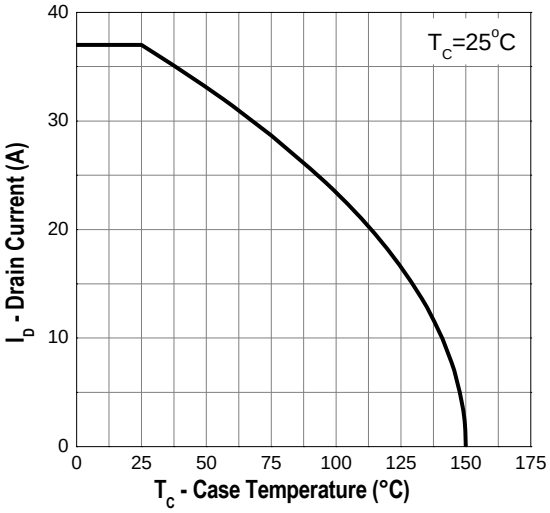


Typical Operating Characteristics (Cont.)

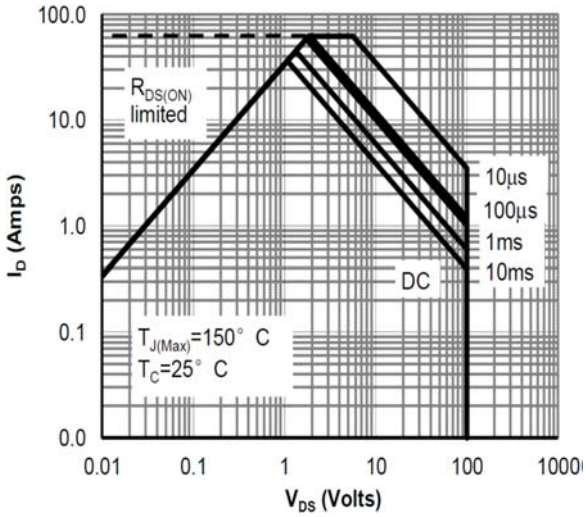
Power Dissipation



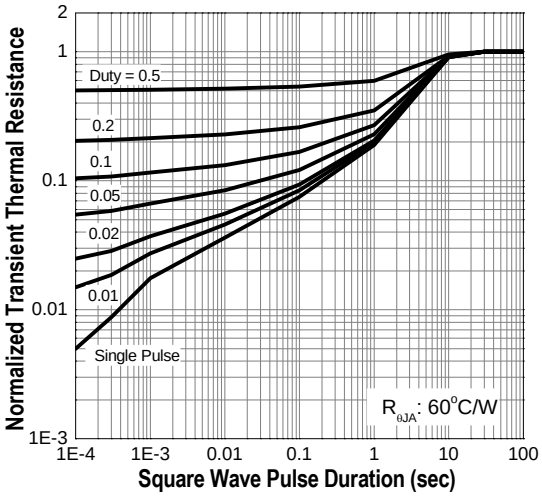
Drain Current



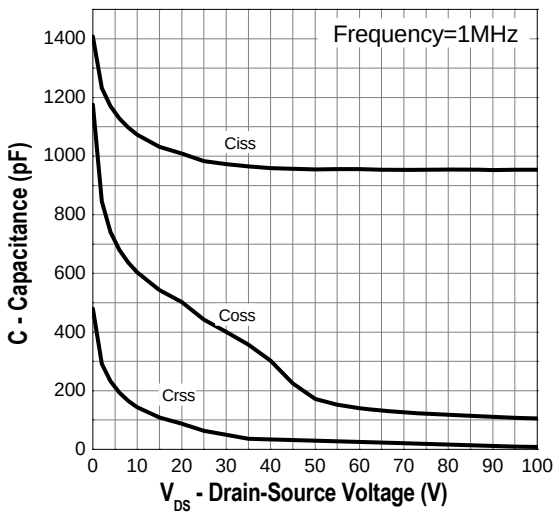
Safe Operation Area



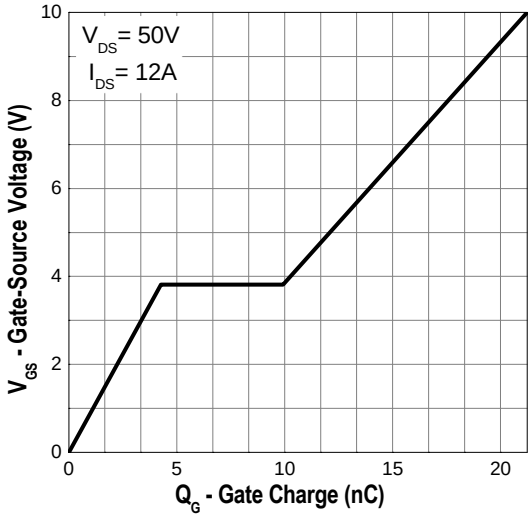
Transient Thermal Impedance



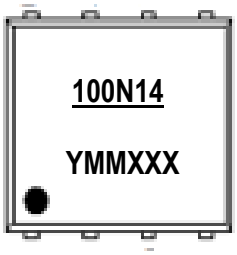
Capacitance



Gate Charge



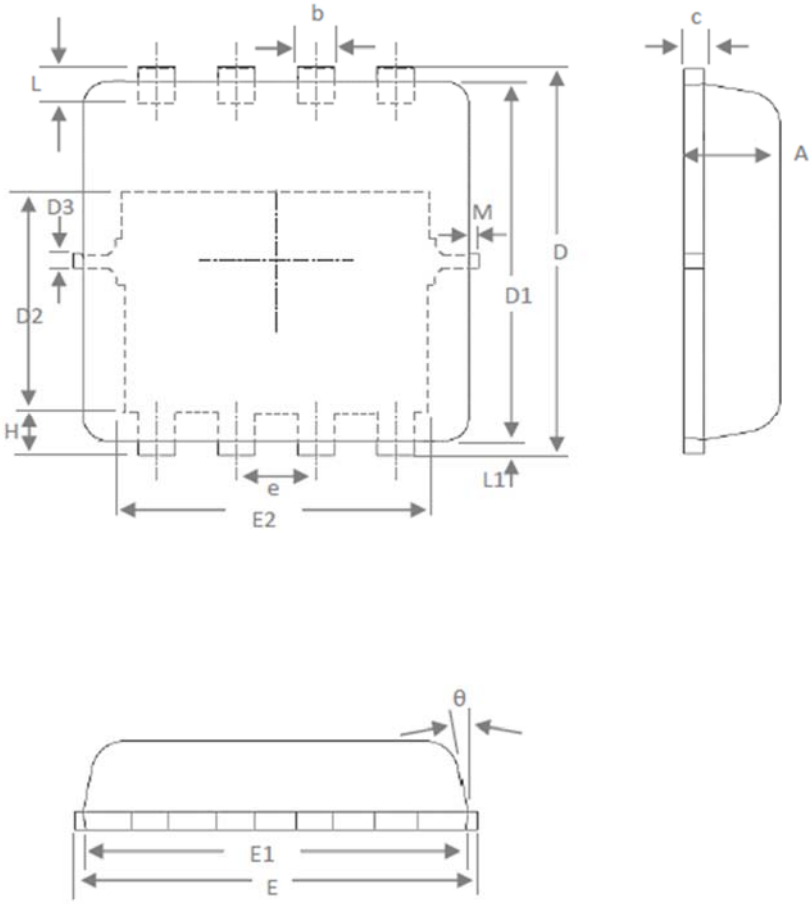
Marking Information

PDFN 3.3x3.3-8L (E)	Marking Rule
Laser Marking  	Line 1：Device 100N14 Line 2：Date Code YMMXXX Y：Year Code MM：Month Code XXX：Serial Number Year Code Description As Below

Year Code Description

Year Code	Year	
0	2010	2020
1	2011	2021
2	2012	2022
3	2013	2023
4	2014	2024
5	2015	2025
6	2016	2026
7	2017	2027
8	2018	2028
9	2019	2029

Package of Dimension

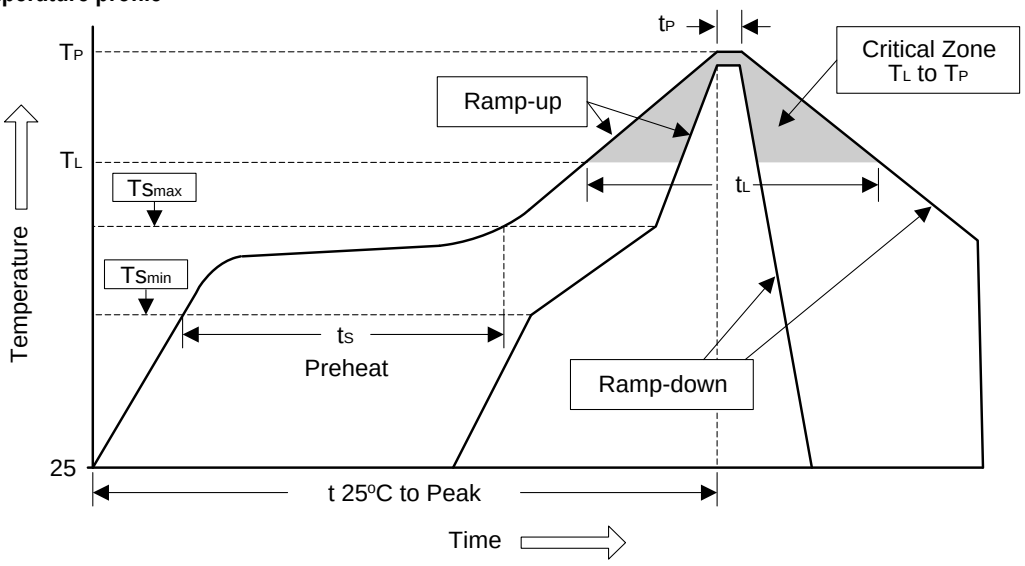


Symbol	Min	Nor	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	-	0.13	-
E	3.00	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	-	0.13	-
θ	-	10°	12°
M	-	-	0.15

Soldering Methods for Silicongear's Products

1. Storage environment: Temperature=10°C to 35°C Humidity=65%±15%
2. Reflow soldering of surface-mount devices

Figure 1: Temperature profile



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	<3°C/sec	<3°C/sec
Preheat - Temperature Min (Ts_{min}) - Temperature Max (Ts_{max}) - Time (min to max) (ts)	 100°C 150°C 60 to 120 sec	 150°C 200°C 60 to 180 sec
Tsmax to T_L - Ramp-up Rate	 <3°C/sec	 <3°C/sec
Time maintained above: - Temperature (T_L) - Time (t_L)	 183°C 60 to 150 sec	 217°C 60 to 150 sec
Peak Temperature (T_P)	240°C +0/-5°C	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10 to 30 sec	20 to 40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25°C to Peak Temperature	<6 minutes	<8 minutes

3. Flow (wave) soldering (solder dipping)

Products	Peak Temperature	Dipping Time
Pb devices.	245°C ±5°C	5sec ±1sec
Pb-Free devices.	260°C +0/-5°C	5sec ±1sec

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