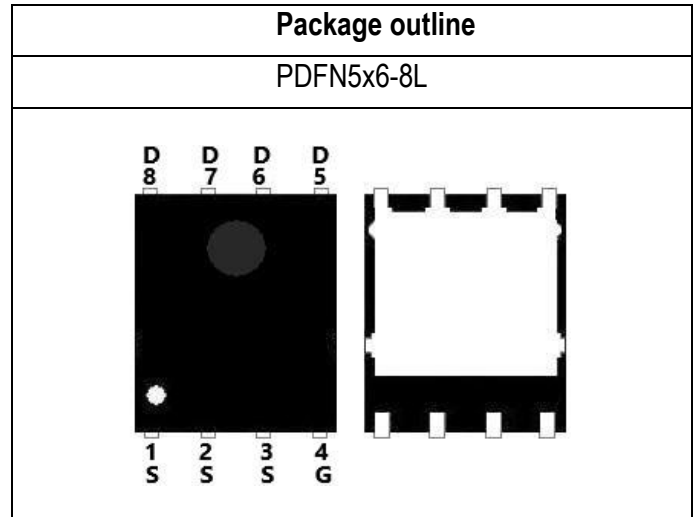


Key parameter	Value	Unit
$V_{(BR)DSS}$ min.	100	V
$R_{DS(ON)}$ max. $V_{GS}=10V$	5.6	m $\Omega$
$I_D$	67	A
$V_{GS(TH)}$ Typ.	3.0	V
$C_{iss}$ Typ.	3740	pF
$Q_g$ 10V Typ.	68.5	nC
$E_{AS}$	36.1	mJ



### Description

These devices used double-gate structure of MOSFET to provide excellent electrical parameter. There is high speed switching capacity, low  $R_{DS(ON)}$  resistance, low gate charge and stable characteristics for these devices. Moreover, it is a helpful choose for raise efficiency or reduce consumption in circuit. These features combine to be an advantage design for use in wide variety of application including converter and inverter design.

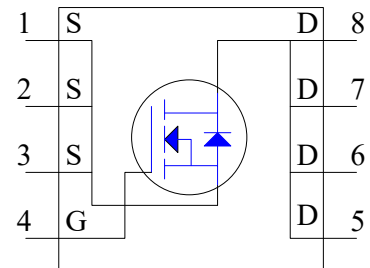
### Features

- ◇ Fast switch capacity
- ◇ Low  $R_{DS(ON)}$  resistance
- ◇ Low input capacitance
- ◇ With voltage logic level driving characteristics
- ◇ Pb-free lead plating; RoHS compliant

### Potential application

- AC to DC adaptor
- DC to DC Converter
- Power Switch Mode Supply
- Synchronous Rectifier for Power Delivery
- Network equipment and display power supply unit

### Symbol and Pin assignment



### Order Information

Item	Description
1. Order Code	DG100N15HQ
2. Part Number	DG100N15HQ
3. Package Type	PDFN5x6-8L
4. Package Code	Q
5. Packing Type	Tape & Reel
6. Quantity in Pack	2,500
7. RoHS Status	Halogen-Free

## Content

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2.	Thermal Resistance Ratings -----	3
3.	Electrical Characteristics -----	4
4.	Typical Operating Characteristics Diagram -----	5-7
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6.	Package of Dimension -----	9
7.	Land pattern (Footprint) -----	9
8.	Appendix -----	10-11

## 1. Absolute Maximum Ratings ( $T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current-Continuous <sup>Note 1</sup>	$T_C=25^\circ\text{C}$	$I_D$	67	A
	$T_C=100^\circ\text{C}$		42.4	A
Drain Current-Continuous <sup>Note 2</sup>	$T_A=25^\circ\text{C}$	$I_D$	17.6	A
	$T_A=70^\circ\text{C}$		14.1	A
Drain Current-Pulsed <sup>Note 3</sup>	$T_A=25^\circ\text{C}$	$I_{DM}$	200	A
Avalanche Current		$I_{AR}$	26.9	A
Single Pulse Avalanche Energy <sup>Note 4</sup>		$E_{AS}$	36.1	mJ
Maximum Power Dissipation	$T_C=25^\circ\text{C}$	$P_D$	42.9	W
	$T_C=100^\circ\text{C}$		17.1	W
	$T_A=25^\circ\text{C}$		2.9	W
	$T_A=70^\circ\text{C}$		1.9	W
	Derate Factor Above $T_C=25^\circ\text{C}$		0.34	W/ $^\circ\text{C}$
Max. Operating Junction Temperature		$T_J$	150	$^\circ\text{C}$
Operating and Storage Temperature Range		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

## 2. Thermal Resistance Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal resistance, Junction-Case	$R_{\theta JC-N}$	Please refer to Note 5	-	-	2.91	$^\circ\text{C}/\text{W}$
Thermal resistance, Junction-Ambient	$R_{\theta JA-N}$	Please refer to Note 5	-	-	41.81	$^\circ\text{C}/\text{W}$

### Notes:

- Limited by silicon chip capability and  $R_{\theta JC-N}$  junction-to-case thermal resistance.
- The maximum current rating is limited by package and  $R_{\theta JA-N}$  junction-to-ambient thermal resistance.
- Must be ensure junction temperature does not exceed 150-degree C. (Pulse Width  $\leq 380\mu\text{s}$ , Duty  $\leq 2\%$ )
- Limited by  $T_{Jmax}$ , starting  $T_J=25^\circ\text{C}$ ,  $L=0.1\text{mH}$ ,  $R_g=25\Omega$ ,  $I_D=26.9\text{A}$ ,  $V_{GS}=10\text{V}$ .
- The value of thermal resistance is measured with the single device mounted on 1 inch<sup>2</sup> FR-4 PCB with 2 oz. copper under a still air environment temperature is  $25^\circ\text{C}$  based on JEDEC standard JESD51-14 and JESD51-2a. Thermal resistance obtained depends on the user's specific board design and given application.

### 3. Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

STATIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>DS</sub> =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V	-	-	1	μA
		V <sub>DS</sub> =100V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C	-	-	100	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA

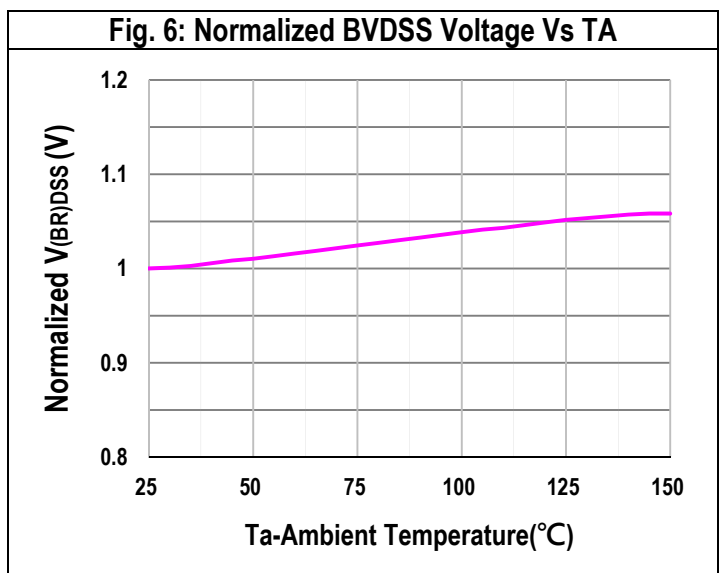
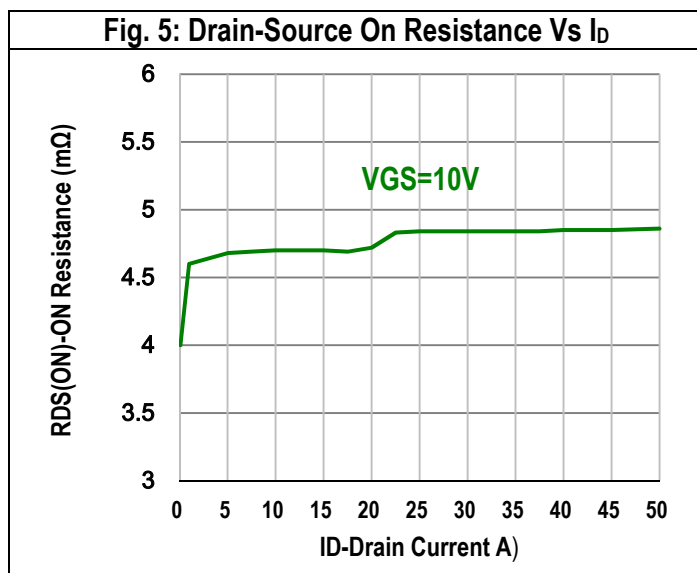
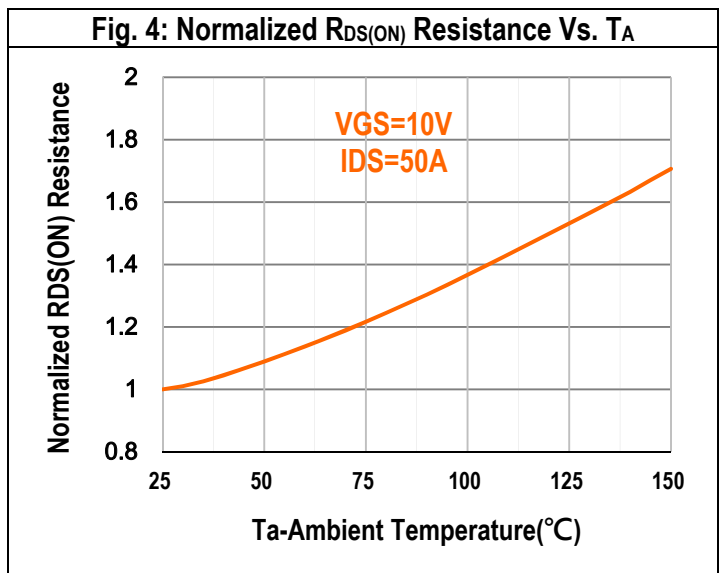
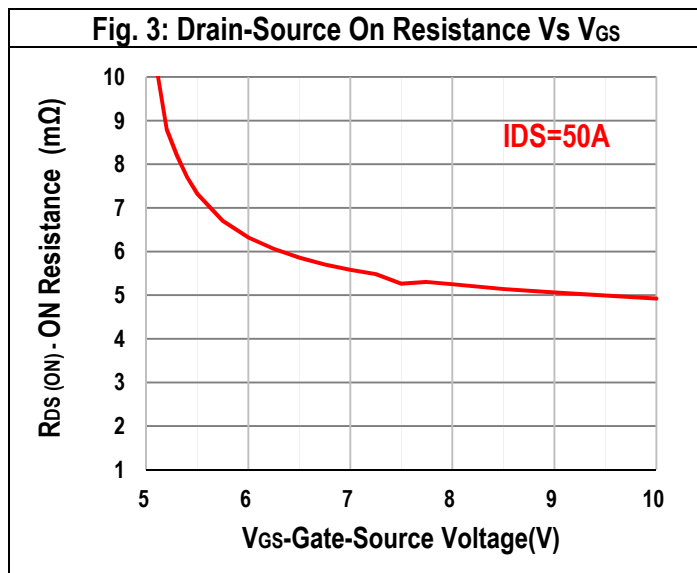
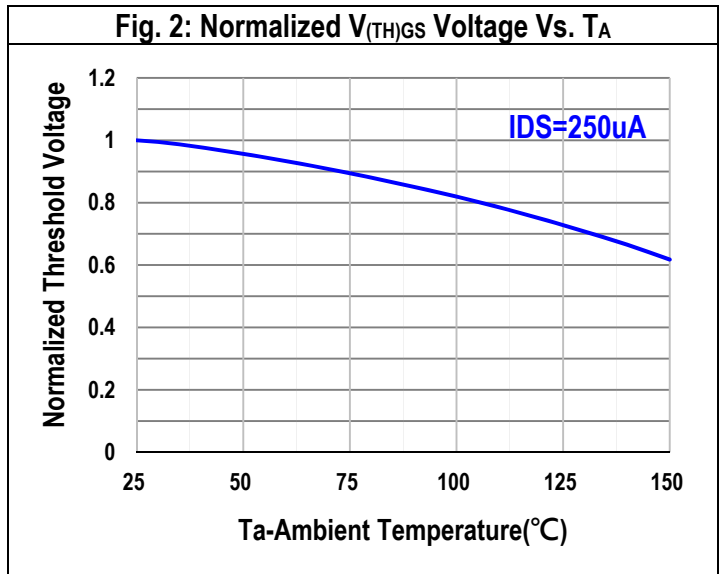
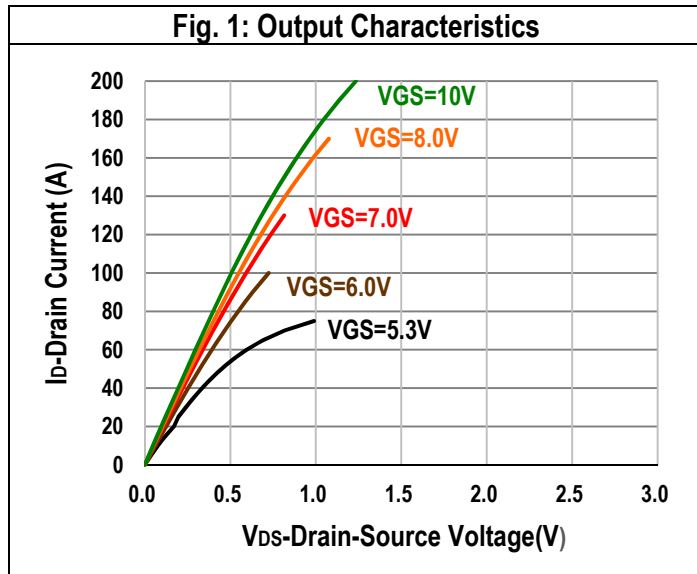
STATIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>DS</sub> =250μA	2.7	3.0	3.3	V
Drain-Source On-State Resistance	R <sub>D(S)ON</sub>	V <sub>GS</sub> =10V, I <sub>DS</sub> =50A	-	4.9	5.6	mΩ
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	-	1.3	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =5V, I <sub>DS</sub> =20A	-	27.7	-	S

DYNAMIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C <sub>iss</sub>	V <sub>DD</sub> =100V, V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, F=1MHz	-	3740	-	pF
Output Capacitance	C <sub>oss</sub>	V <sub>DD</sub> =100V, V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, F=1MHz	-	570	-	pF
Reverse Transfer Capacitance	C <sub>rss</sub>	V <sub>DD</sub> =100V, V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, F=1MHz	-	13.0	-	pF
Turn-On Delay Time	T <sub>d(on)</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =10V, I <sub>DS</sub> =50A, R <sub>GEN</sub> =3.0Ω	-	18.5	-	nS
Rise Time	T <sub>r</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =10V, I <sub>DS</sub> =50A, R <sub>GEN</sub> =3.0Ω	-	48.6	-	nS
Turn-Off Delay Time	T <sub>d(off)</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =10V, I <sub>DS</sub> =50A, R <sub>GEN</sub> =3.0Ω	-	42.2	-	nS
Fall Time	T <sub>f</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =10V, I <sub>DS</sub> =50A, R <sub>GEN</sub> =3.0Ω	-	26.6	-	nS

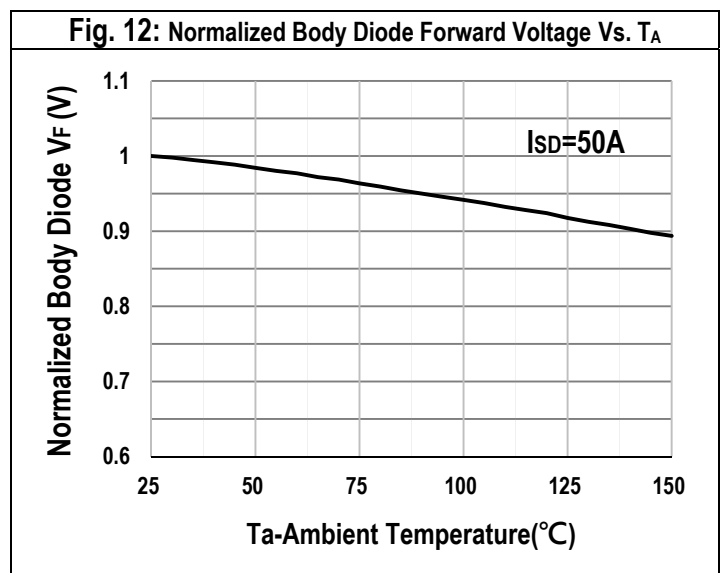
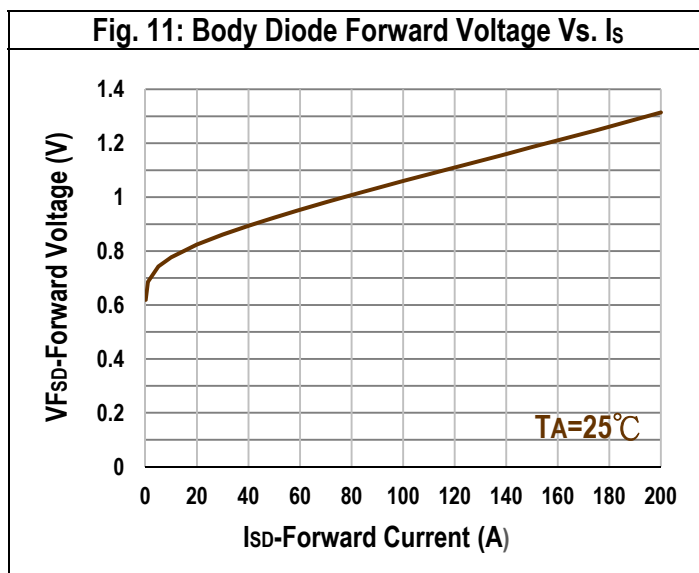
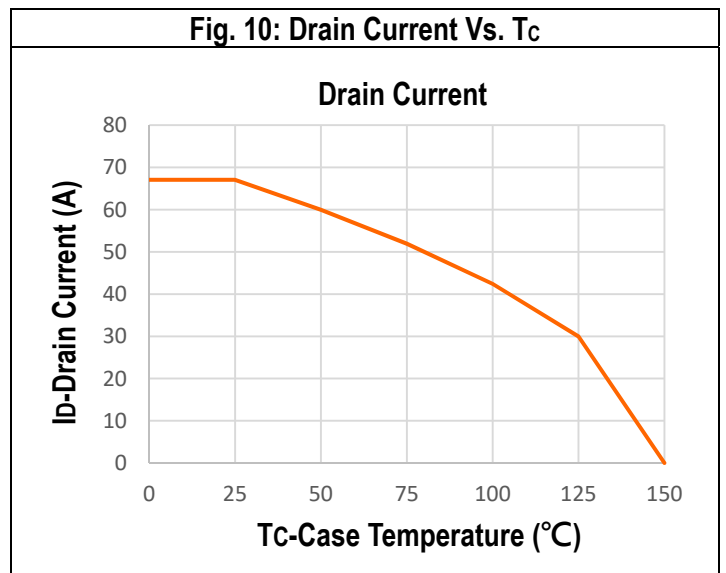
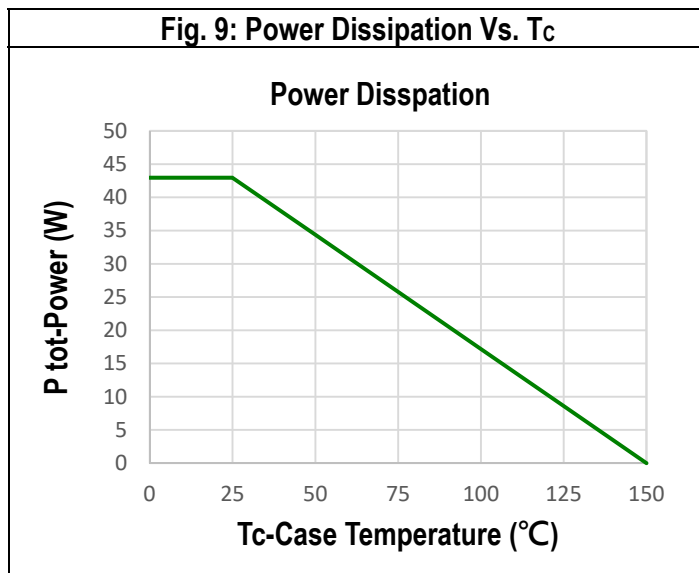
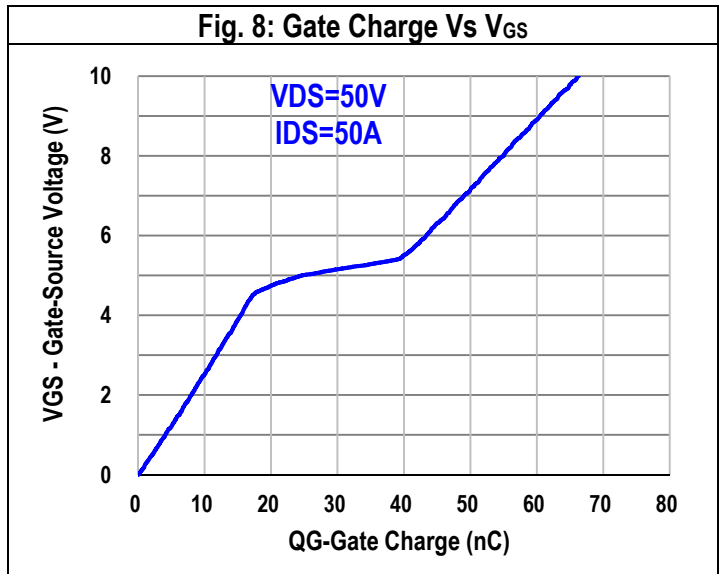
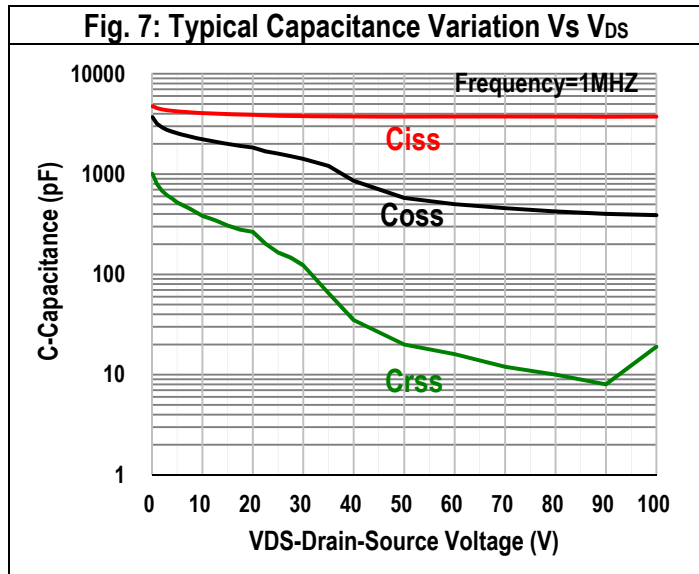
GATE CHARGE CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gate to Source Gate Charge	Q <sub>gs</sub>	V <sub>DD</sub> =50V, I <sub>D</sub> =50A, V <sub>GS</sub> =0 to 10V	-	19.5	-	nC
Gate charge at threshold	Q <sub>g(th)</sub>	V <sub>DD</sub> =50V, I <sub>D</sub> =50A, V <sub>GS</sub> =0 to 10V	-	10.9	-	nC
Gate to Drain Charge	Q <sub>gd</sub>	V <sub>DD</sub> =50V, I <sub>D</sub> =50A, V <sub>GS</sub> =0 to 10V	-	22.0	-	nC
Switching charge	Q <sub>sw</sub>	V <sub>DD</sub> =50V, I <sub>D</sub> =50A, V <sub>GS</sub> =0 to 10V	-	30.5	-	nC
Gate charge total	Q <sub>g 10V</sub>	V <sub>DD</sub> =50V, I <sub>D</sub> =50A, V <sub>GS</sub> =0 to 10V	-	68.5	-	nC
Gate plateau voltage	V <sub>plateau</sub>	V <sub>DD</sub> =50V, I <sub>D</sub> =50A, V <sub>GS</sub> =0 to 10V	-	5.1	-	V
Gate charge total, sync. FET (Q <sub>g</sub> - Q <sub>gd</sub> )	Q <sub>g(sync)</sub>	V <sub>DS</sub> =0.1V, V <sub>GS</sub> =0 to 10V	-	46.5	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Body Diode continuous forward current	I <sub>S</sub>	T <sub>C</sub> =25°C	-	-	67	A
Body Diode pulse current	I <sub>SM</sub>	T <sub>C</sub> =25°C	-	-	200	A
Body Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =30A	-	0.92	1.0	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	V <sub>DD</sub> =50V, I <sub>F</sub> =50A, di/dt=100A/μs	-	49.7	-	nS
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	V <sub>DD</sub> =50V, I <sub>F</sub> =50A, di/dt=100A/μs	-	52.4	-	nC
Body Diode Reverse Recovery Current	I <sub>rm</sub>	V <sub>DD</sub> =50V, I <sub>F</sub> =50A, di/dt=100A/μs	-	2.0	-	A

## 4. Typical Operating Characteristics Diagram



4. Typical Operating Characteristics Diagram



4. Typical Operating Characteristics Diagram

Fig. 13: Safe Operation Area

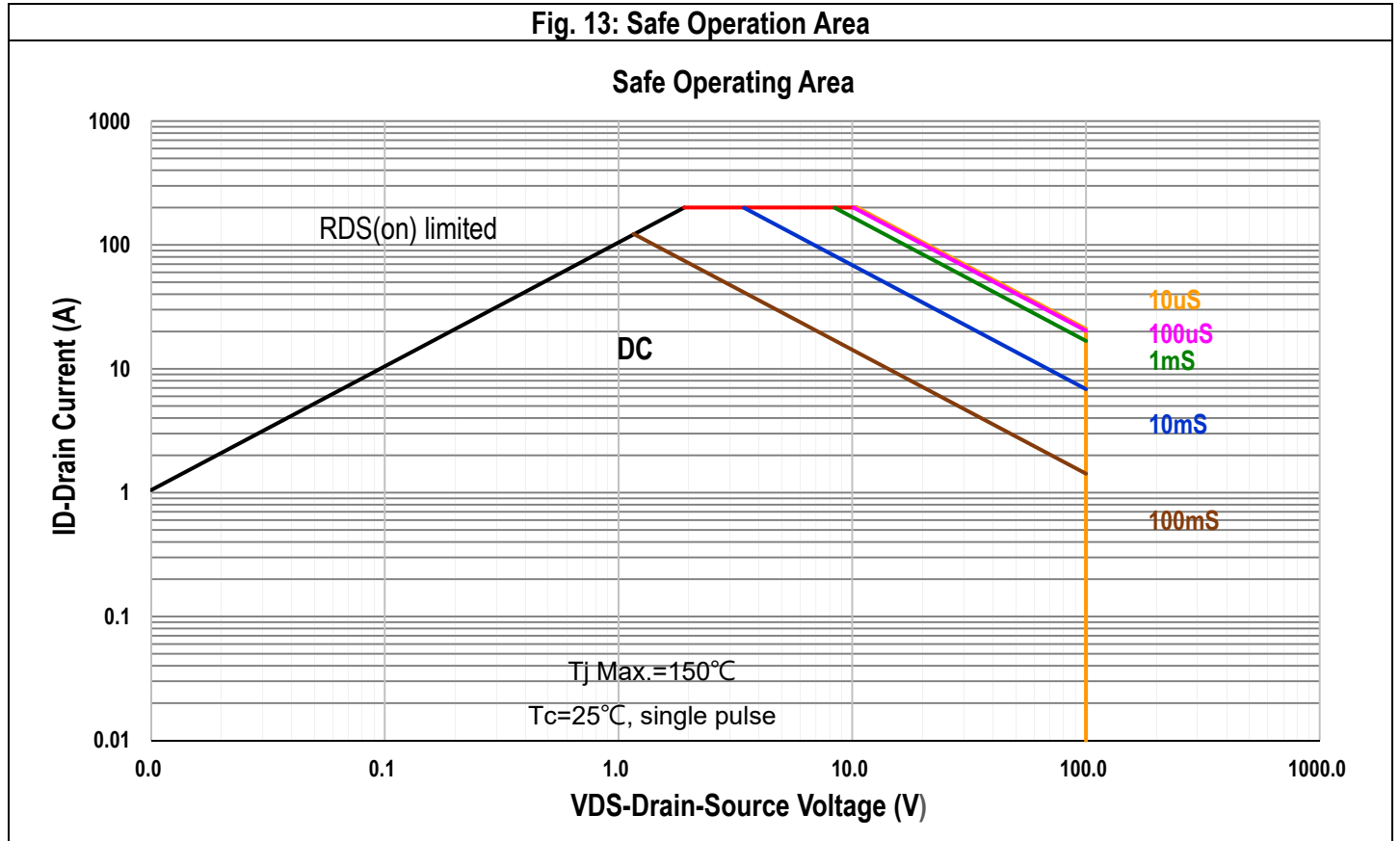
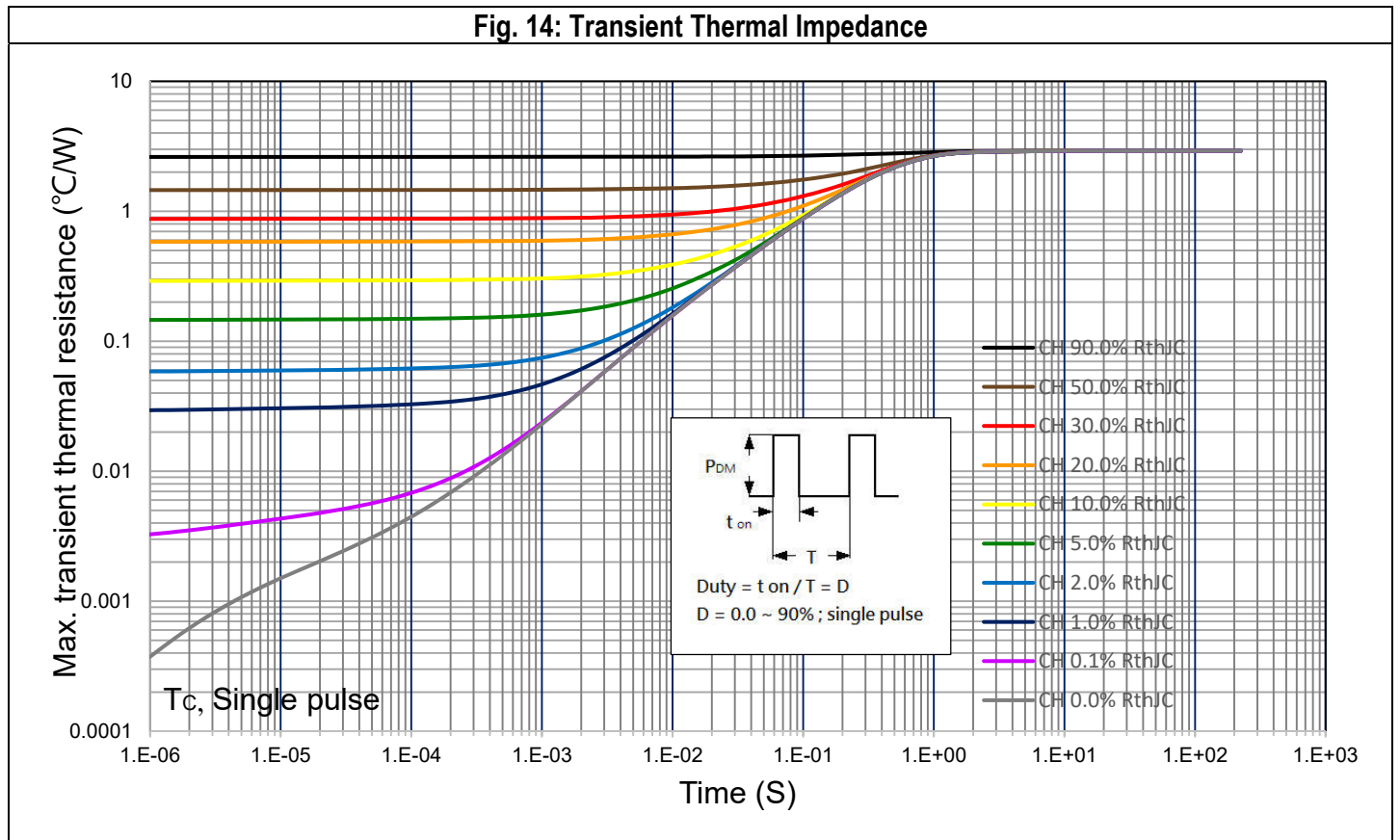



Fig. 14: Transient Thermal Impedance



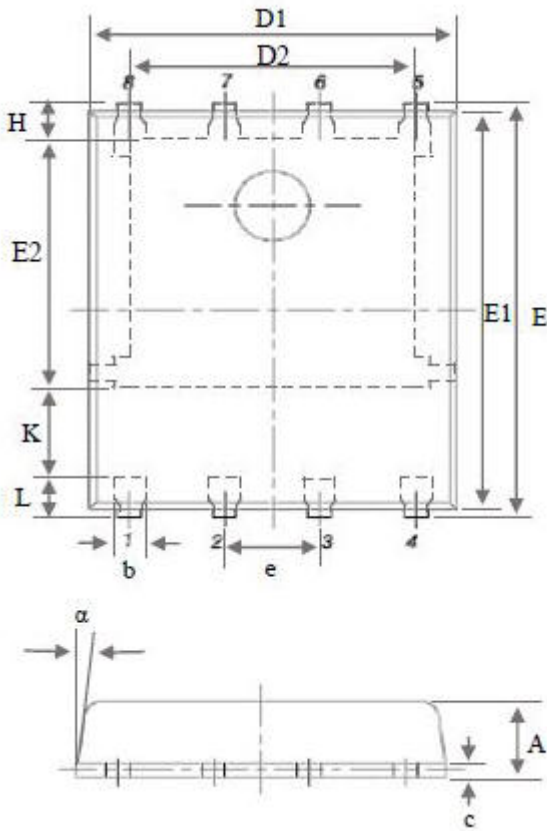
## 5. Marking Information

PDFN 5x6-8L (Q)	Marking Rule
<p>Laser Marking</p> 	<p><u>Line 1</u> : Device DG100N15HQ</p> <p><u>Line 2</u> : Date Code YYMMXXX</p> <p>YY : Year Code MM : Month Code XXX : Serial Number</p>



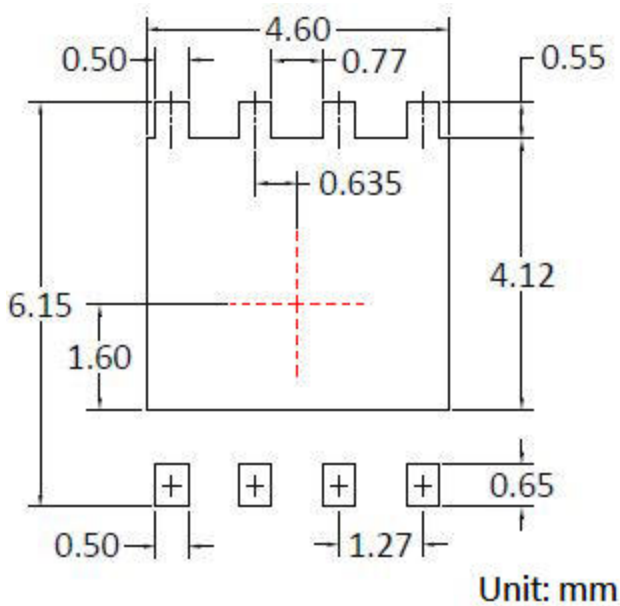
## 6. Package of Dimension

Package type: PDFN 5x6-8L



Symbol	Min	Nor	Max
A	0.90	1.04	1.17
b	0.33	0.42	0.51
C	0.06	0.20	0.35
D1	4.80	5.10	5.40
D2	3.61	3.96	4.31
E	5.90	6.03	6.15
E1	5.65	5.75	5.85
E2	3.30	3.54	3.78
e	1.27 BSC		
H	0.38	0.50	0.61
L	0.38	0.55	0.71
L1	0.05	0.15	0.25

## 7. Land pattern (Footprint)

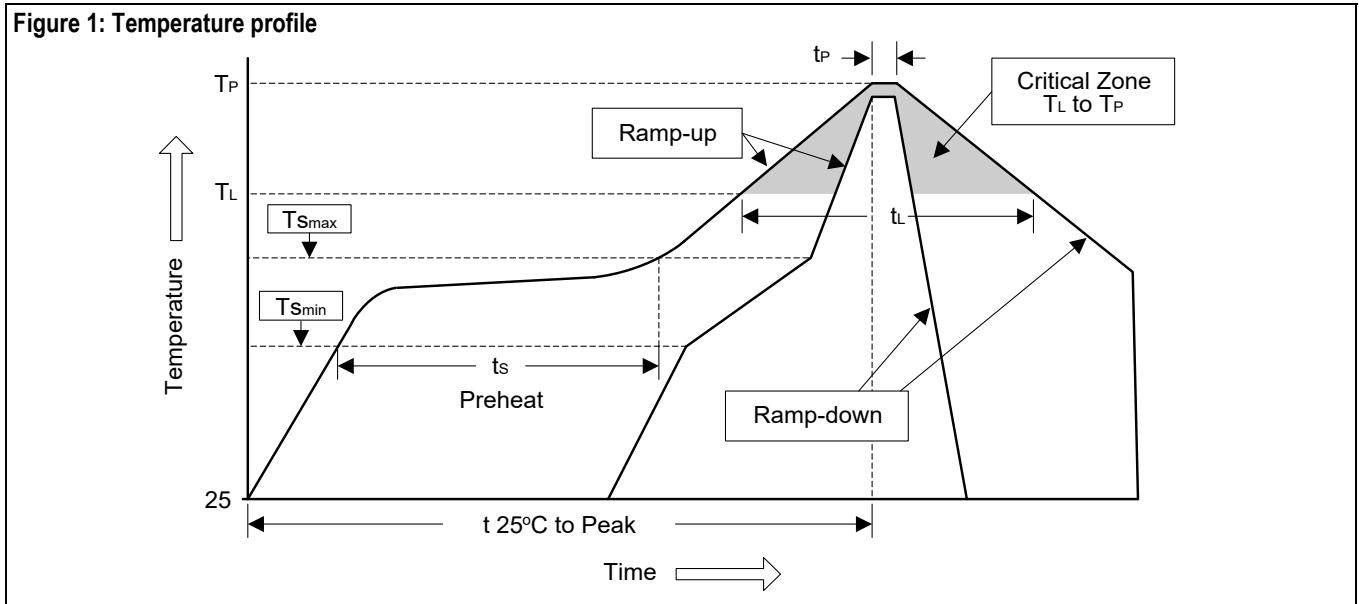


- Note 1: Land pattern (Footprint) design is for reference only.
- Note 2: Package body sizes exclude mold flash and burrs.
- Note 3: Dimension is measured in gauge plane.
- Note 4: Tolerance 0.1mm unless otherwise specified.

## 8. Appendix-A

### Soldering Methods for Silicongear's Products (Just for SMD type of device)

- Storage environment: Temperature=10°C to 35°C Humidity=65%±15%
- Reflow soldering of surface-mount devices



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (TL to TP)	<3°C/sec	<3°C/sec
Preheat		
- Temperature Min (T <sub>smmin</sub> )	100°C	150°C
- Temperature Max (T <sub>smmax</sub> )	150°C	200°C
- Time (min to max) (ts)	60 to 120 sec	60 to 180 sec
T <sub>smmax</sub> to TL		
- Ramp-up Rate	<3°C/sec	<3°C/sec
Time maintained above:		
- Temperature (TL)	183°C	217°C
- Time (t <sub>L</sub> )	60 to 150 sec	60 to 150 sec
Peak Temperature (TP)	240°C +0/-5°C	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10 to 30 sec	20 to 40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25°C to Peak Temperature	<6 minutes	<8 minutes

### 3. Flow (wave) soldering (solder dipping)

Products	Peak Temperature	Dipping Time
Pb devices.	245°C ±5°C	5sec ±1sec
Pb-Free devices.	260°C +0/-5°C	5sec ±1sec

**8. Appendix-B****Important Notice****© Silicongear Corporation**

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