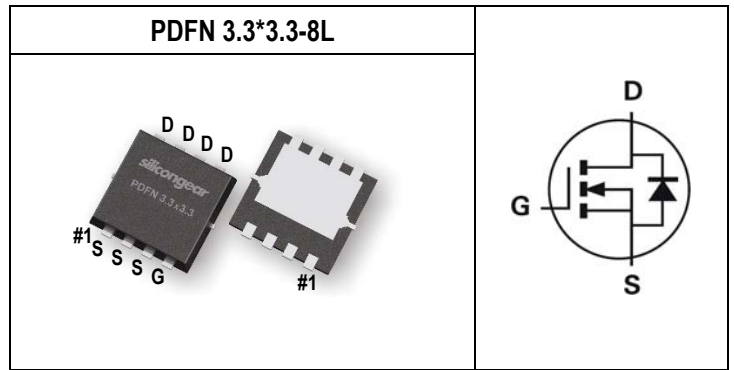


Parameter	Value	Unit
V_{DSS}	100	V
$R_{DS(ON) \max.} V_{GS}=10V$	27	m Ω
$R_{DS(ON) \max.} V_{GS}=4.5V$	31	m Ω
I_D	24	A
Q_g	59	nC
Q_{gd}	9	nC
Q_{sw}	17.4	nC



Features	Application
<ul style="list-style-type: none"> • Low On-Resistance • Low Miller Charge • Fully Characterized Capacitance and Avalanche • Pb-free lead plating; RoHS compliant 	<ul style="list-style-type: none"> • Motor / Body Load Control • Automotive Systems • Load Switch • DC-DC converters and Off-line UPS

Ordering Information

Ordering Code	RoHS Status	Package	Package Code	Packing	Quantity
SG100N07E	Halogen-Free	PDFN 3.3*3.3-8L	E	Tape & Reel	5,000

Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous ^{Note 1}	I_D	$T_C=25^\circ\text{C}$	24
		$T_C=100^\circ\text{C}$	15
Drain Current-Pulsed ^{Note 2}	I_{DM}	49	A
Avalanche Current	I_{AR}	16	A
Single Pulse Avalanche Energy ^{Note 3}	E_{AS}	13	mJ
Maximum Power Dissipation	P_D	$T_C=25^\circ\text{C}$	48
		$T_C=100^\circ\text{C}$	19
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Ambient ^{Note 4}	$R_{\theta JA}$	Steady State	-	-	32	$^\circ\text{C/W}$
Thermal resistance, Junction-to-Case ^{Note 4}	$R_{\theta JC}$	Steady State	-	-	1.56	$^\circ\text{C/W}$

Notes:

- Limited by silicon chip capability and junction temperature.
- Must be ensure junction temperature does not exceed 150-degree C. (Pulse Width $\leq 100\mu\text{s}$, Duty $\leq 2\%$)
- Limited by $T_{J\max}$, starting $T_J=25^\circ\text{C}$, $L=0.1\text{mH}$, $R_g=25\Omega$, $I_D=25\text{A}$, $V_{GS}=10\text{V}$.
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 in still air.

Electrical Characteristics (T_J=25°C unless otherwise noted)

STATIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _{DS} =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
		V _{DS} =100V, V _{GS} =0V, T _J =125°C	-	-	100	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA

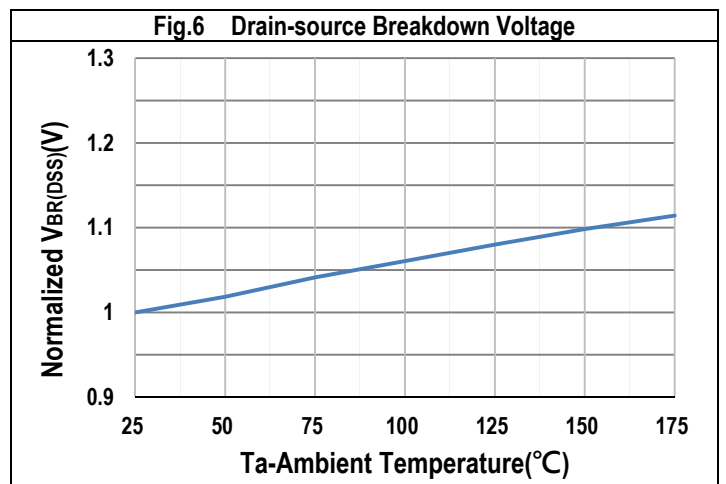
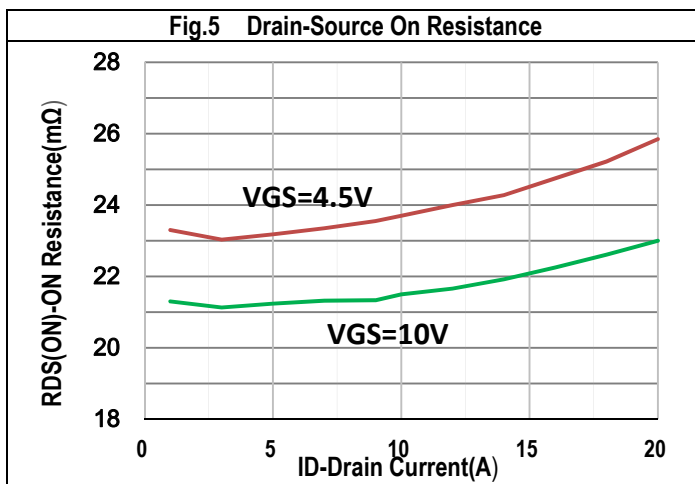
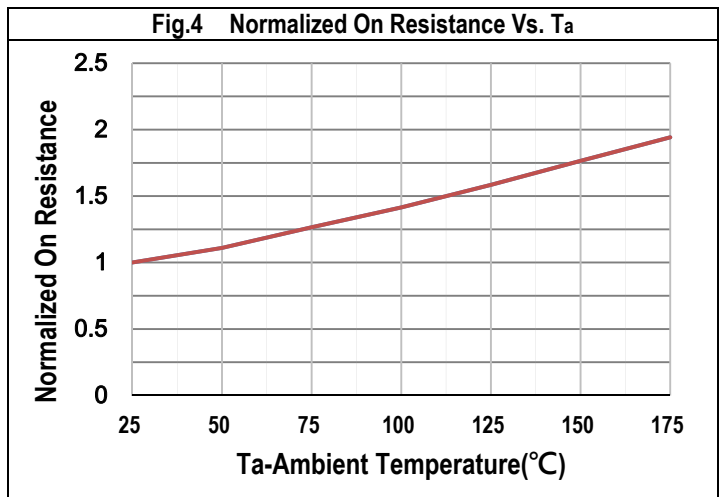
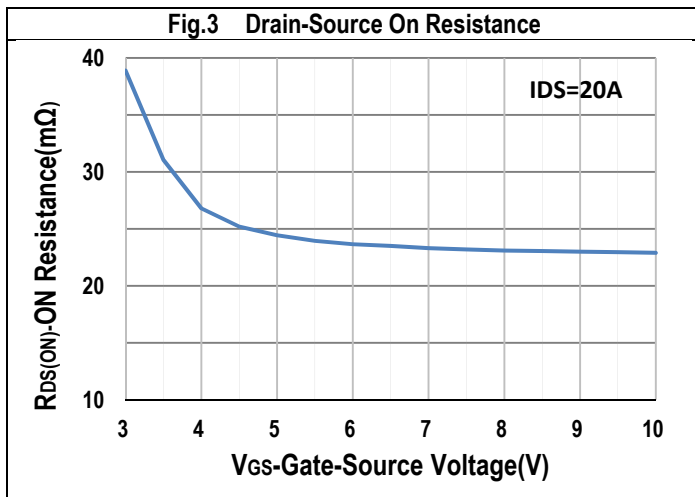
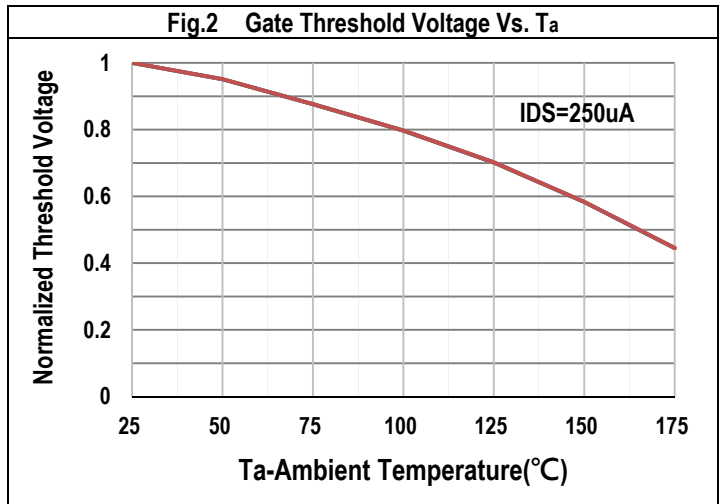
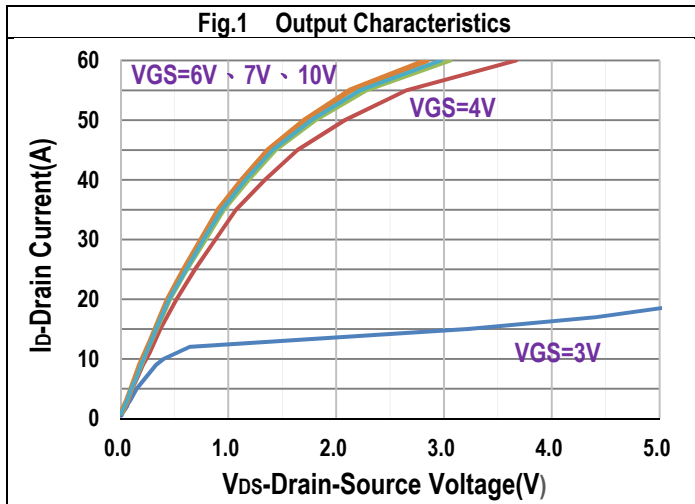
STATIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _{DS} =250μA	1.2	1.7	2.4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _{DS} =10A	-	22	27	mΩ
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _{DS} =6A	-	24	31	mΩ
Gate Resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz	-	0.5	1	Ω
Forward Transconductance	g _{fs}	V _{DS} =5V, I _{DS} =20A	-	19	-	S

DYNAMIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	3205	-	pF
Output Capacitance	C _{oss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	94	-	pF
Reverse Transfer Capacitance	C _{rss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	55	-	pF
Turn-On Delay Time	T _{d(on)}	V _{DS} =50V, V _{GS} =10V, I _{DS} =20A, R _{GEN} =3Ω	-	11	-	ns
Rise Time	t _r	V _{DS} =50V, V _{GS} =10V, I _{DS} =20A, R _{GEN} =3Ω	-	26	-	ns
Turn-Off Delay Time	T _{d(off)}	V _{DS} =50V, V _{GS} =10V, I _{DS} =20A, R _{GEN} =3Ω	-	34	-	ns
Fall Time	t _f	V _{DS} =50V, V _{GS} =10V, I _{DS} =20A, R _{GEN} =3Ω	-	25	-	ns

GATE CHARGE CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gate to Source Gate Charge	Q _{gs}	V _{DD} =50V, I _D =20A, V _{GS} =0 to 10V	-	14.6	-	nC
Gate charge at threshold	Q _{g(th)}	V _{DD} =50V, I _D =20A, V _{GS} =0 to 10V	-	6.2	-	nC
Gate to Drain Charge	Q _{gd}	V _{DD} =50V, I _D =20A, V _{GS} =0 to 10V	-	9	-	nC
Switching charge	Q _{sw}	V _{DD} =50V, I _D =20A, V _{GS} =0 to 10V	-	17.4	-	nC
Gate charge total	Q _g	V _{DD} =50V, I _D =20A, V _{GS} =0 to 10V	-	59	-	nC
Gate charge total	Q _g	V _{DD} =50V, I _D =20A, V _{GS} =0 to 4.5V	-	32	-	nC
Gate plateau voltage	V _{plateau}	V _{DD} =50V, I _D =20A, V _{GS} =0 to 10V	-	3.8	-	V
Gate charge total, sync. FET (Q _g - Q _{gd})	Q _{g(sync)}	V _{DS} =0.1V, V _{GS} =0 to 10V	-	50	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Diode continuous forward current (Body Diode)	I _S	T _C =25°C	-	-	24	A
Diode pulse current (Body Diode)	I _{SM}	T _C =25°C	-	-	49	A
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =1A	-	0.7	1	V
Body Diode Reverse Recovery Time	t _{rr}	V _{DD} =50V, I _F =20A, di/dt=200A/μs	-	23	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}	V _{DD} =50V, I _F =20A, di/dt=200A/μs	-	59	-	nC

Typical Operating Characteristics



Typical Operating Characteristics (Cont.)

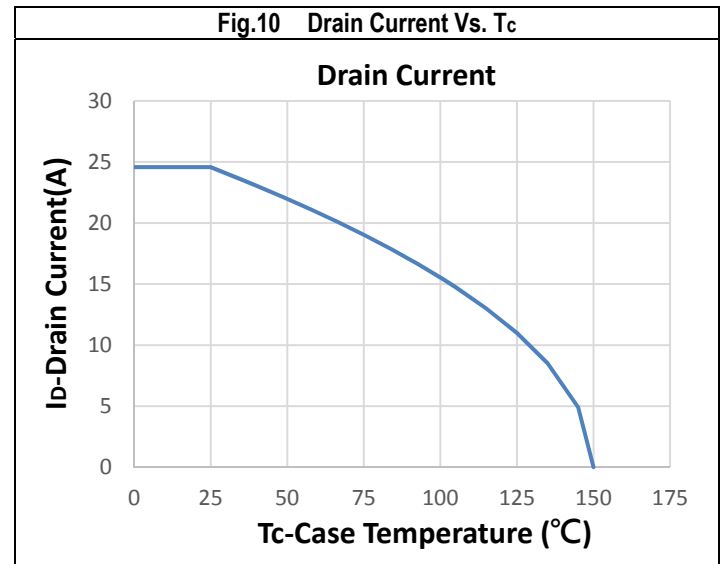
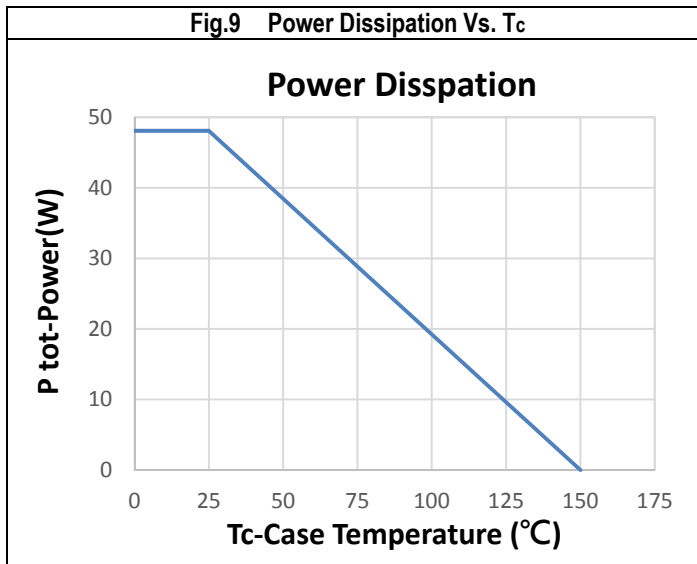
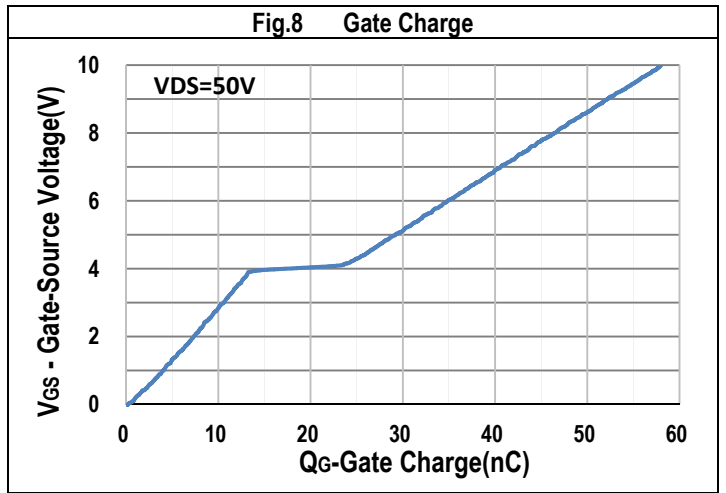
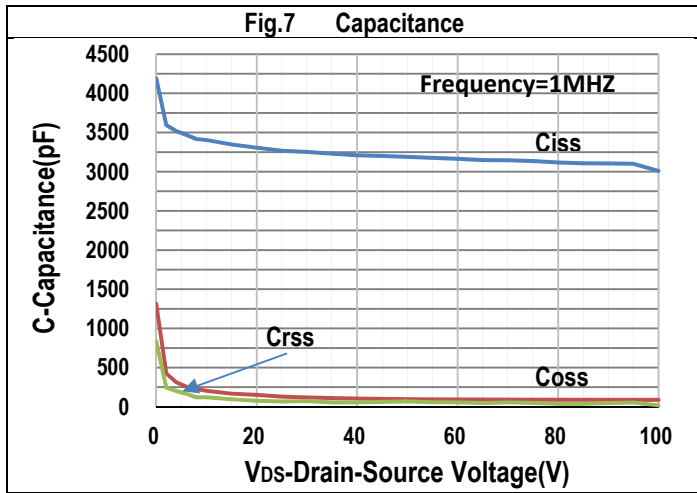


Fig.11 Safe Operation Area

Safe Operating Area

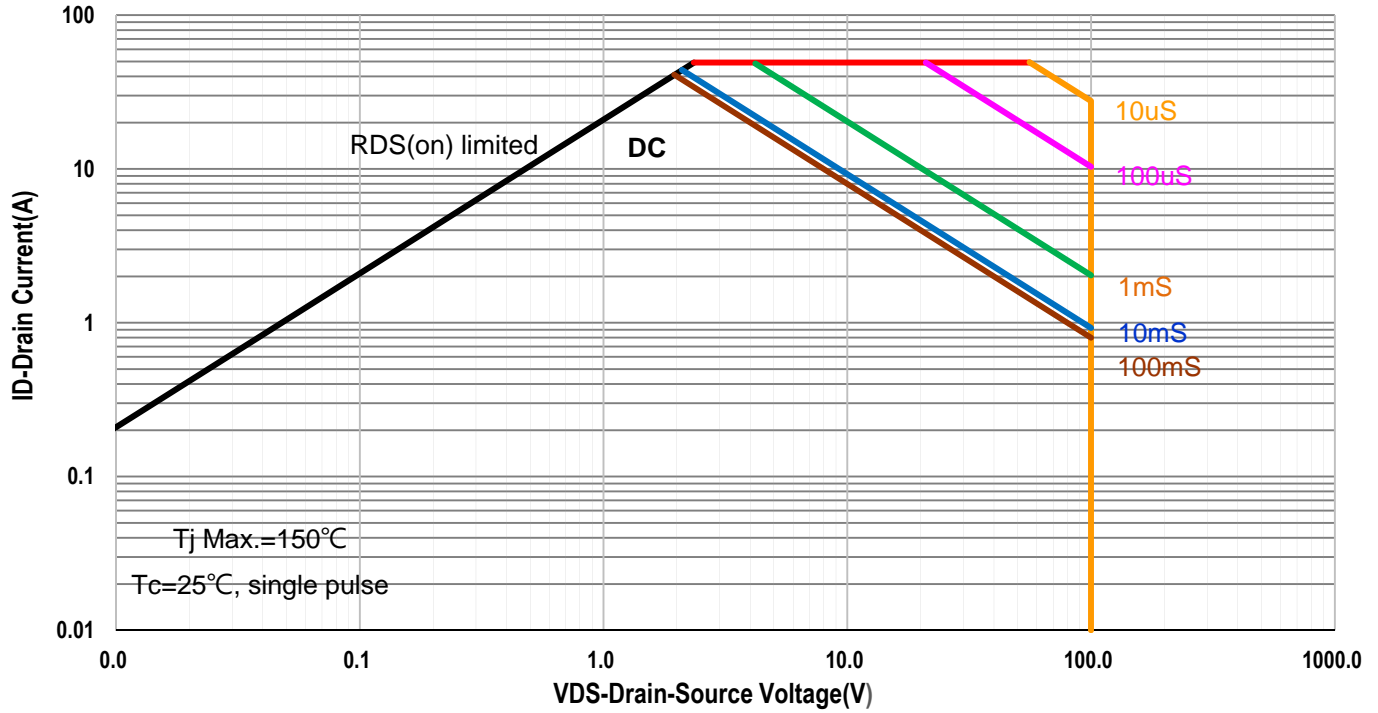
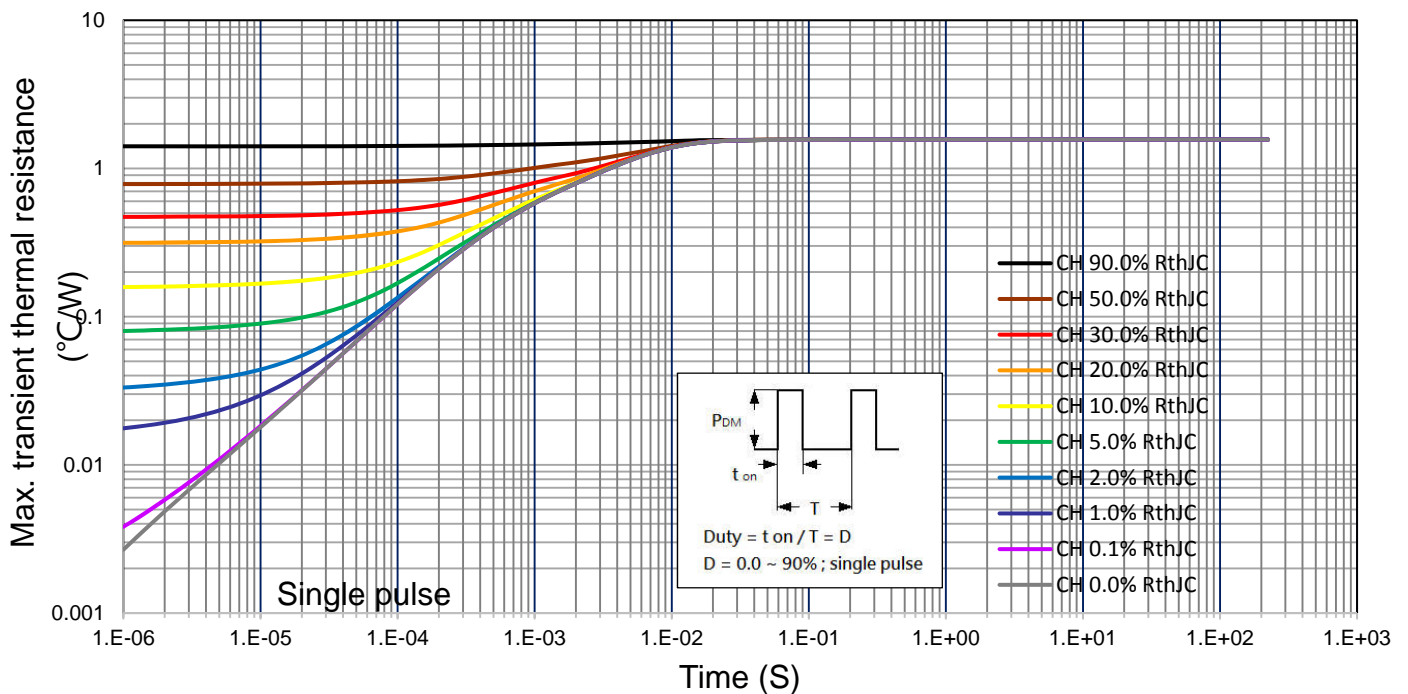
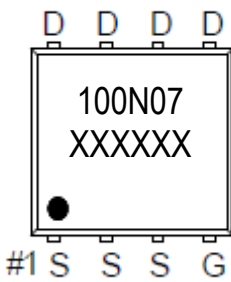


Fig.12 Transient Thermal Impedance



Marking Information

PDFN 3.3*3.3-8L	Marking Rule
<p>Laser Marking</p> 	<p><u>Line 1</u> : Device 100N07</p> <p><u>Line 2</u> : Date Code YMMXXX</p> <p>Y : Year Code MM : Month Code XXX : Serial Number</p>

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