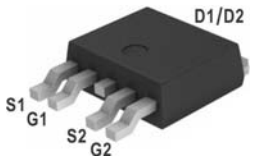
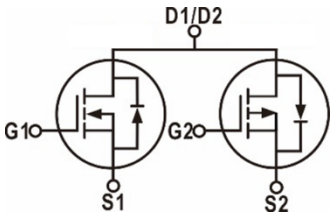
SGD100C03H

100V /-100V Complementary, Power MOSFET

Parameter	N channel	P channel	Unit
V_{DSS}	100	-100	V
$R_{DS\ (ON)}$ max. VGS=10V	116.4	277.9	mΩ
$R_{DS\ (ON)}$ max. VGS=4.5V	123.8	300.7	mΩ
I_D	12.3	-7.6	A
$Q_{g\ 10V}$	16.2	17.4	nC
Q_{gd}	2	2.2	nC
Q_{SW}	3.8	4.1	pF

TO-252-4L(Dual)





Features

- Low On-Resistance
- Low Input Capacitance
- Low Miller Charge
- Low Input / Output Leakage
- Pb-free lead plating; RoHS compliant

Application

- Motor / Body Load Control
- Automotive Systems
- Load Switch

Ordering Information

Ordering Code	RoHS Status	Package	Package Code	Packing	Quantity
SGD100C03H	Halogen-Free	TO-252-4L(Dual)	H	Tape & Reel	2,500

Absolute Maximum Ratings (T_J=25°C unless otherwise noted)

Parameter		Symbol	N channel	P channel	Unit
Drain-Source Voltage		V_{DS}	100	-100	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Drain Current-Continuous Note 1	T_C=25°C	I_D	12.3	-7.6	A
	T_C=100°C		7.7	-4.8	A
Drain Current-Continuous Note 2	T_A=25°C	I_D	2.6	-1.8	A
	T_A=70°C		2.1	-1.4	A
Drain Current-Pulsed Note 3	T_A=25°C	I_{DM}	14.0	-9.0	A
Avalanche Current		I_{AR}	2.1	-4.2	A
Single Pulse Avalanche Energy Note 4		E_{AS}	0.23	1.0	mJ
Maximum Power Dissipation	T_C=25°C	P_D	42.0	33.9	W
	T_C=100°C		16.8	13.5	W
	T_A=25°C	P_D	1.9	1.9	W
	T_A=70°C		1.2	1.2	W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal resistance, Junction-Case Note 5	$R_{\theta JC}$	Steady State(N-Channel)	-	-	2.9	°C/W
		Steady State(P-Channel)		-	3.6	°C/W
Thermal resistance, Junction-Ambient Note 5	$R_{\theta JA}$	Steady State(N-Channel)		-	57.5	°C/W
		Steady State(P-Channel)	-	-	61.5	°C/W

Notes:

1. Limited by silicon chip capability and $R_{\theta JC}$ junction-to-case thermal resistance.
2. The maximum current rating is limited by package and $R_{\theta JA}$ junction-to-ambient thermal resistance.
3. Must be ensure junction temperature does not exceed 150-degree C. (Pulse Width ≦ 100uS, Duty ≦ 10%)
4. Limited by TJmax, starting T_J = 25°C, L = 0.1mH, R_g = 25Ω, V_{GS} = 10V.
5. The The value of thermal resistance is measured with the single device mounted on 1 inch^2 FR-4 PCB with 2 oz. copper under a still air environment temperature is 25℃ based on JEDEC standard JESD51-14 and JESD51-2a. Thermal resistance obtained depends on the user's specific board design and given application.

N-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

STATIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_{DS}=250µA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	µA
		V_{DS}=100V, V_{GS}=0V, T_J=125°C	-	-	100	µA
Gate-Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA

STATIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_{DS}=250µA	1.2	1.6	2.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_{DS}=2A	-	97.0	116.4	mΩ
		V_{GS}=4.5V, I_{DS}=1A	-	103.0	123.8	mΩ
Gate Resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz	-	1.3	-	Ω
Forward Transconductance	g_{fs}	V_{DS}=5V, I_{DS}=2A	-	6.8	-	S

DYNAMIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Input Capacitance	C_{iss}	V_{DD}=100V,V_{DS}=50V, V_{GS}=0V, f=1MHz	-	914.9	-	pF
Output Capacitance	C_{oss}	V_{DD}=100V,V_{DS}=50V, V_{GS}=0V, f=1MHz	-	25.4	-	pF
Reverse Transfer Capacitance	C_{rss}	V_{DD}=100V,V_{DS}=50V, V_{GS}=0V, f=1MHz	-	18.2	-	pF
Turn-On Delay Time	$T_{d(on)}$	V_{DS}=50V, V_{GS}=10V, I_{DS}=2A, R_{GEN}=3Ω	-	6.3	-	nS
Rise Time	t_r	V_{DS}=50V, V_{GS}=10V, I_{DS}=2A, R_{GEN}=3Ω	-	2.2	-	nS
Turn-Off Delay Time	$T_{d(off)}$	V_{DS}=50V, V_{GS}=10V, I_{DS}=2A, R_{GEN}=3Ω	-	17	-	nS
Fall Time	t_f	V_{DS}=50V, V_{GS}=10V, I_{DS}=2A, R_{GEN}=3Ω	-	9.2	-	nS

GATE CHARGE CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Gate to Source Gate Charge	Q_{gs}	V_{DD}=50V, I_D=2A, V_{GS}=0 to 10V	-	3.4	-	nC
Gate charge at threshold	$Q_{g(th)}$	V_{DD}=50V, I_D=2A, V_{GS}=0 to 10V	-	1.6	-	nC
Gate to Drain Charge	Q_{gd}	V_{DD}=50V, I_D=2A, V_{GS}=0 to 10V	-	2	-	nC
Switching charge	Q_{SW}	V_{DD}=50V, I_D=2A, V_{GS}=0 to 10V	-	3.8	-	nC
Gate charge total	$Q_{g\ 10V}$	V_{DD}=50V, I_D=2A, V_{GS}=0 to 10V	-	16.2	-	nC
	$Q_{g\ 4.5V}$	V_{DD}=50V, I_D=2A, V_{GS}=0 to 4.5V	-	7.4	-	nC
Gate plateau voltage	$V_{plateau}$	V_{DD}=50V, I_D=2A, V_{GS}=0 to 10V	-	3.1	-	V
Gate charge total, sync. FET (Q_g- Q_{gd})	$Q_{g(sync)}$	V_{DS}=0.1V, V_{GS}=0 to 10V	-	14.2	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Body Diode continuous forward current	I_S	T_C=25°C	-	-	12.3	A
Body Diode pulse current	I_{SM}	T_C=25°C	-	-	14	A
Body Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=2A	-	0.77	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	V_{DD}=50V, I_F=2A, di/dt=100A/µs	-	15.8	-	nS
Body Diode Reverse Recovery Charge	Q_{rr}	V_{DD}=50V, I_F=2A, di/dt=100A/µs	-	12.1	-	nC

P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

STATIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_{DS}=-250µA	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V, V_{GS}=0V	-	-	-1	µA
		V_{DS}=-100V, V_{GS}=0V, T_J=125°C	-	-	-100	µA
Gate-Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA

STATIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_{DS}=-250µA	-1.3	-1.7	-2.1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_{DS}=-2A	-	231.6	277.9	mΩ
		V_{GS}=-4.5V, I_{DS}=-1A	-	250.6	300.7	mΩ
Gate Resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz	-	14.5	-	Ω
Forward Transconductance	g_{fs}	V_{DS}=-5V, I_{DS}=-2A	-	5.4	-	S

DYNAMIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Input Capacitance	C_{iss}	V_{DD}=-100V, V_{DS}=-50V, V_{GS}=0V, f=1MHz	-	982.0	-	pF
Output Capacitance	C_{oss}	V_{DD}=-100V, V_{DS}=-50V, V_{GS}=0V, f=1MHz	-	30.0	-	pF
Reverse Transfer Capacitance	C_{rss}	V_{DD}=-100V, V_{DS}=-50V, V_{GS}=0V, f=1MHz	-	22.8		pF
Turn-On Delay Time	$T_{d(on)}$	V_{DS}=-50V, V_{GS}=-10V, I_{DS}=-2A, R_{GEN}=49.9Ω	-	13.4	-	nS
Rise Time	t_r	V_{DS}=-50V, V_{GS}=-10V, I_{DS}=-2A, R_{GEN}=49.9Ω	-	16.8	-	nS
Turn-Off Delay Time	$T_{d(off)}$	V_{DS}=-50V, V_{GS}=-10V, I_{DS}=-2A, R_{GEN}=49.9Ω	-	159.8	-	nS
Fall Time	t_f	V_{DS}=-50V, V_{GS}=-10V, I_{DS}=-2A, R_{GEN}=49.9Ω	-	48.6	-	nS

GATE CHARGE CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Gate to Source Gate Charge	Q_{gs}	V_{DD}=-50V, I_D=-2A, V_{GS}=0 to -10V	-	3.7	-	nC
Gate charge at threshold	$Q_{g(th)}$	V_{DD}=-50V, I_D=-2A, V_{GS}=0 to -10V	-	1.8	-	nC
Gate to Drain Charge	Q_{gd}	V_{DD}=-50V, I_D=-2A, V_{GS}=0 to -10V	-	2.2	-	nC
Switching charge	Q_{SW}	V_{DD}=-50V, I_D=-2A, V_{GS}=0 to -10V	-	4.1	-	nC
Gate charge total	$Q_{g\ 10V}$	V_{DD}=-50V, I_D=-2A, V_{GS}=0 to -10V	-	17.4	-	nC
	$Q_{g\ 4.5V}$	V_{DD}=-50V, I_D=-2A, V_{GS}=0 to -4.5V	-	7.9	-	nC
Gate plateau voltage	$V_{plateau}$	V_{DD}=-50V, I_D=-2A, V_{GS}=0 to -10V	-	3.2	-	V
Gate charge total, sync. FET (Q_g- Q_{gd})	$Q_{g(sync)}$	V_{DS}=0.1V, V_{GS}=0 to -10V	-	15.2	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Body Diode continuous forward current	I_S	T_C=25°C	-	-	-7.6	A
Body Diode pulse current	I_{SM}	T_C=25°C	-	-	-9	A
Body Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=-2A	-	-0.81	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	V_{DD}=-50V, I_F=-2A, di/dt=100A/µs	-	17.9	-	nS
Body Diode Reverse Recovery Charge	Q_{rr}	V_{DD}=-50V, I_F=-2A, di/dt=100A/µs	-	15.2	-	nC

N-Channel Typical Operating Characteristics

Fig. 1 Output Characteristics

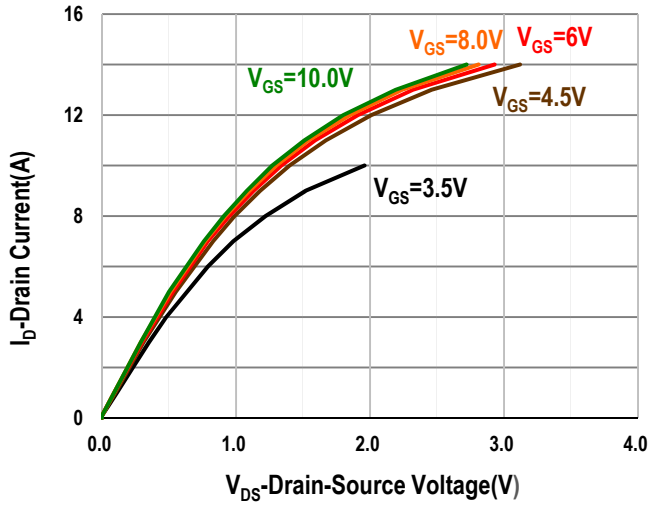


Fig. 2 Gate Threshold Voltage Vs Ta

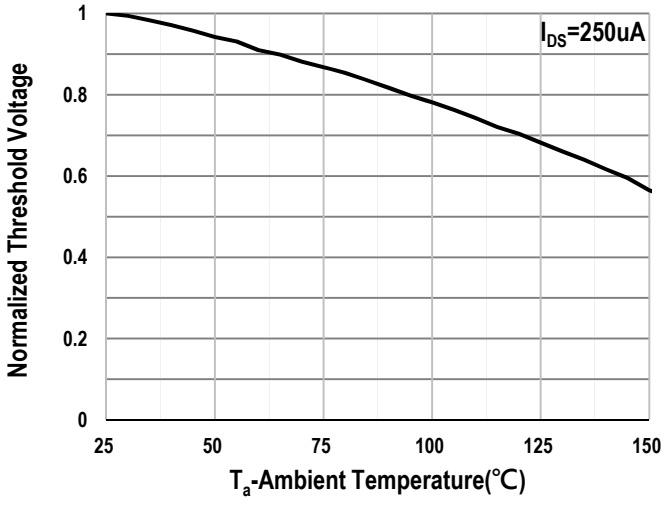


Fig. 3 Drain-Source On Resistance

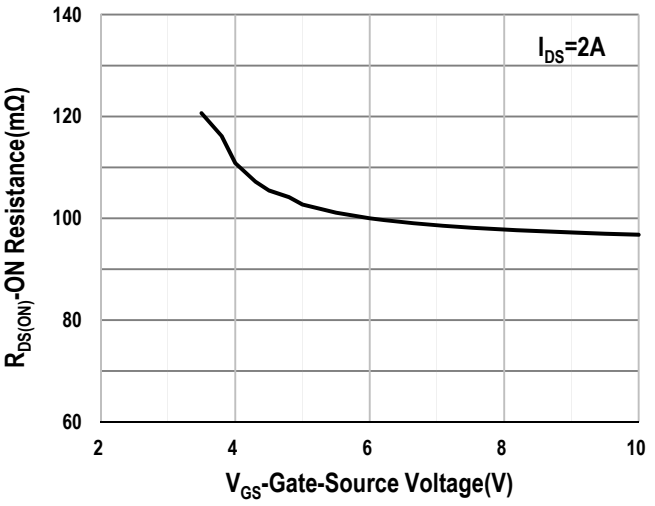


Fig. 4 Normalized On Resistance Vs T_a

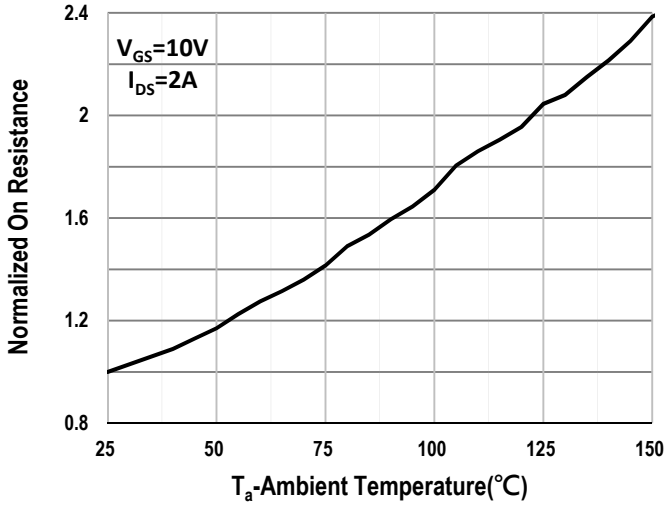


Fig. 5 Drain-Source On Resistance

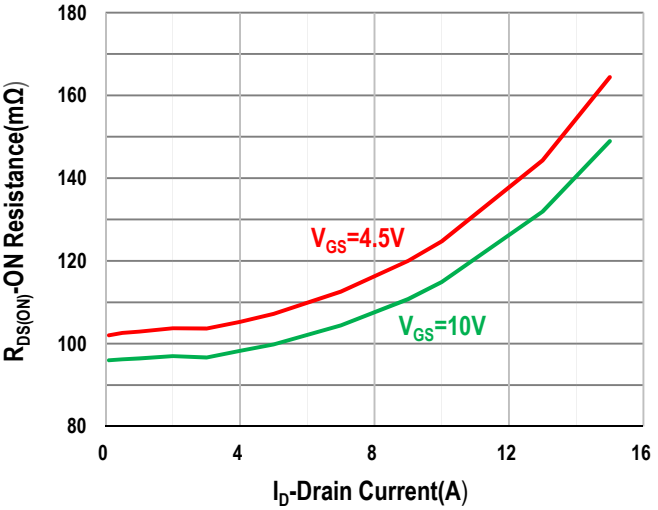
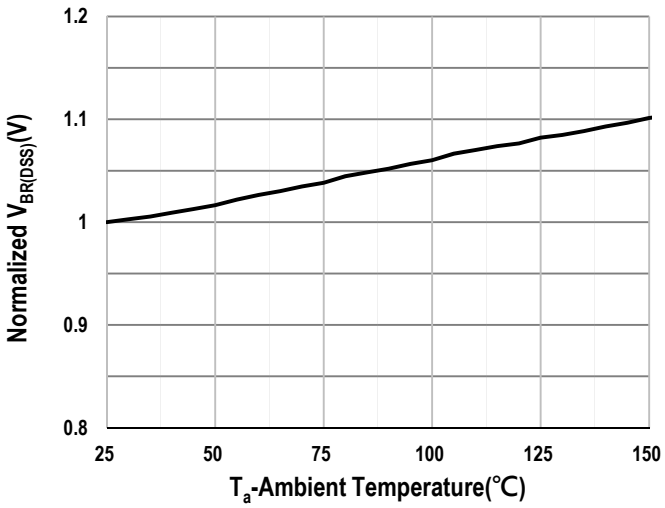


Fig. 6 Drain-source Breakdown Voltage Vs T_a



N-Channel Typical Operating Characteristics

Fig. 7 Capacitance Vs V_{DS}

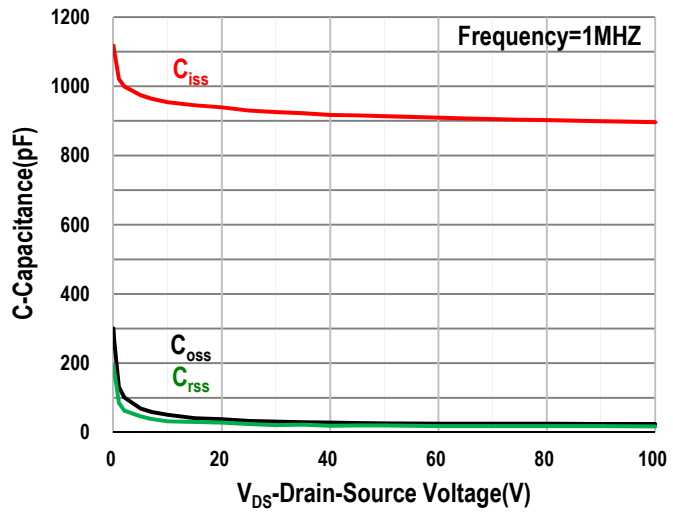


Fig. 8 Gate Charge Vs V_{GS}

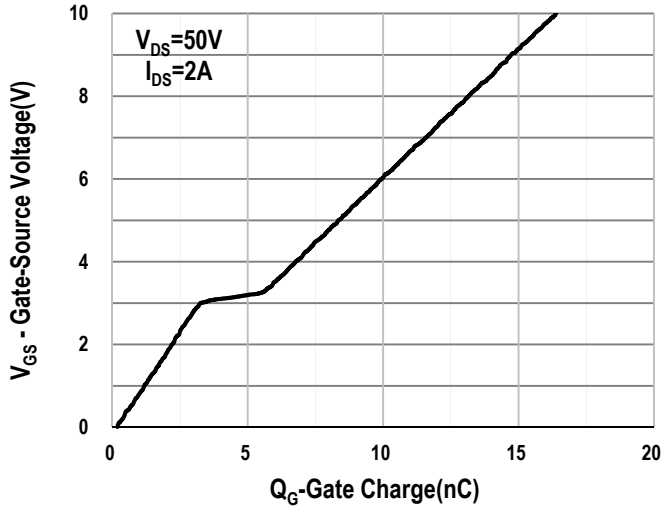


Fig.9 Power Dissipation Vs Tc

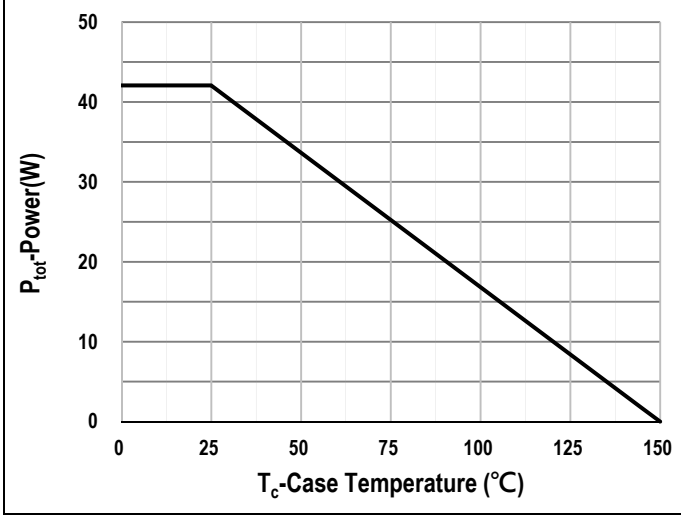


Fig.10 Drain Current Vs Tc

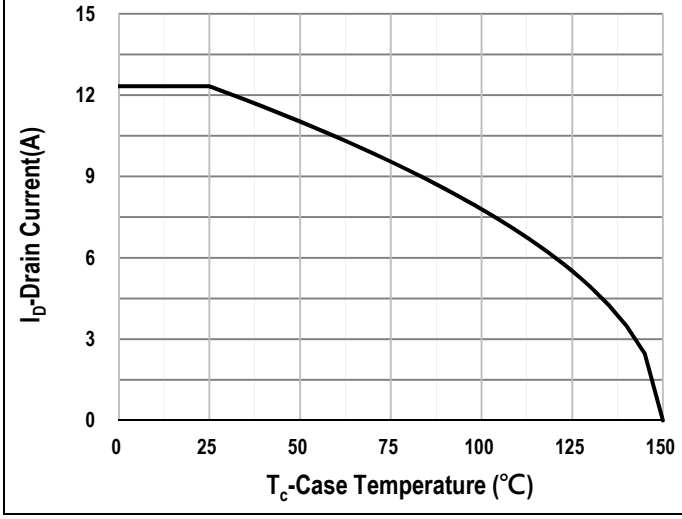


Fig. 11 Body Diode Forward Voltage Vs I_{SD}

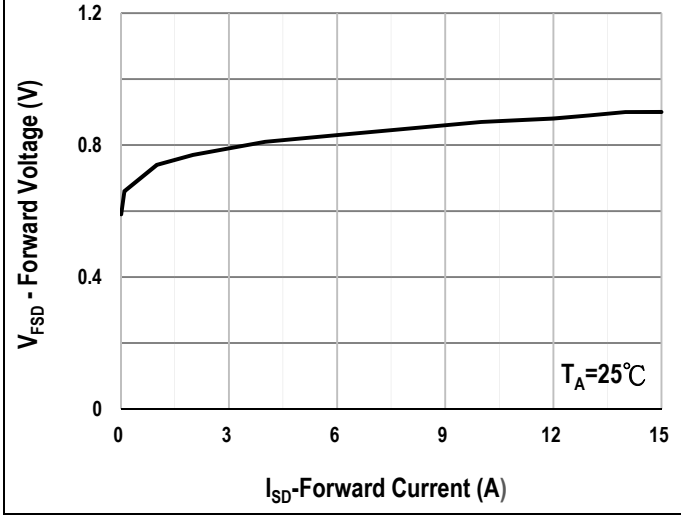


Fig. 12 Body Diode Forward Voltage Vs T_A

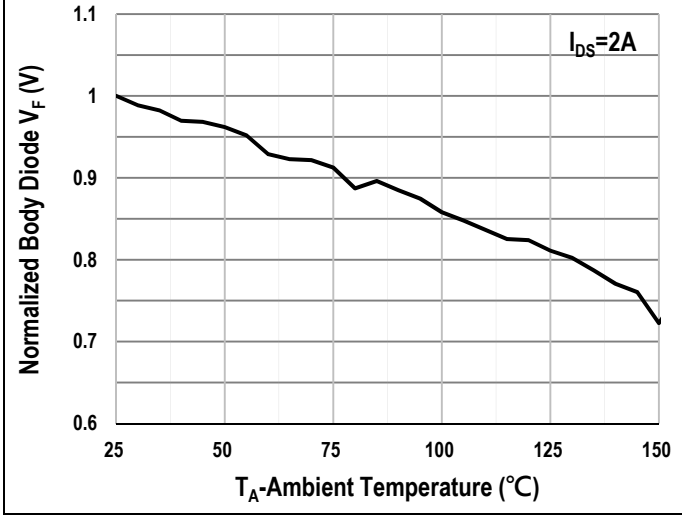


Fig. 13 Safe Operation Area

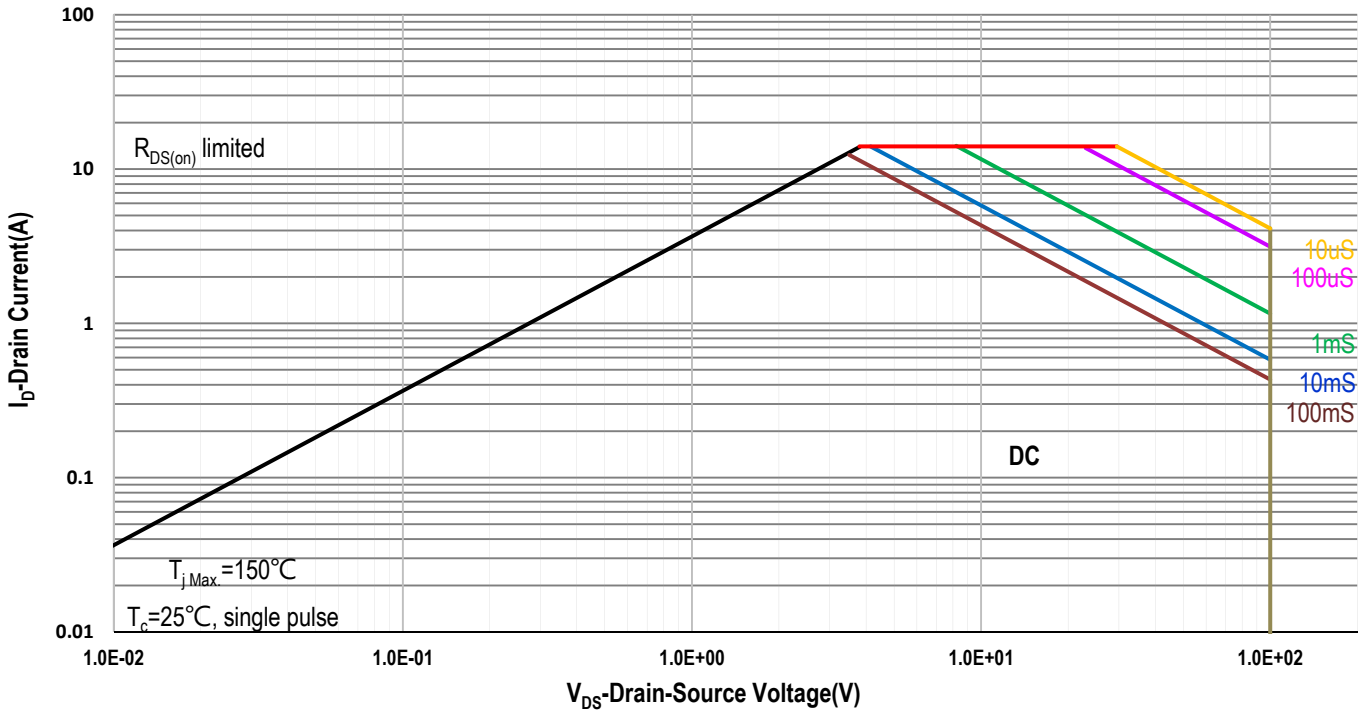
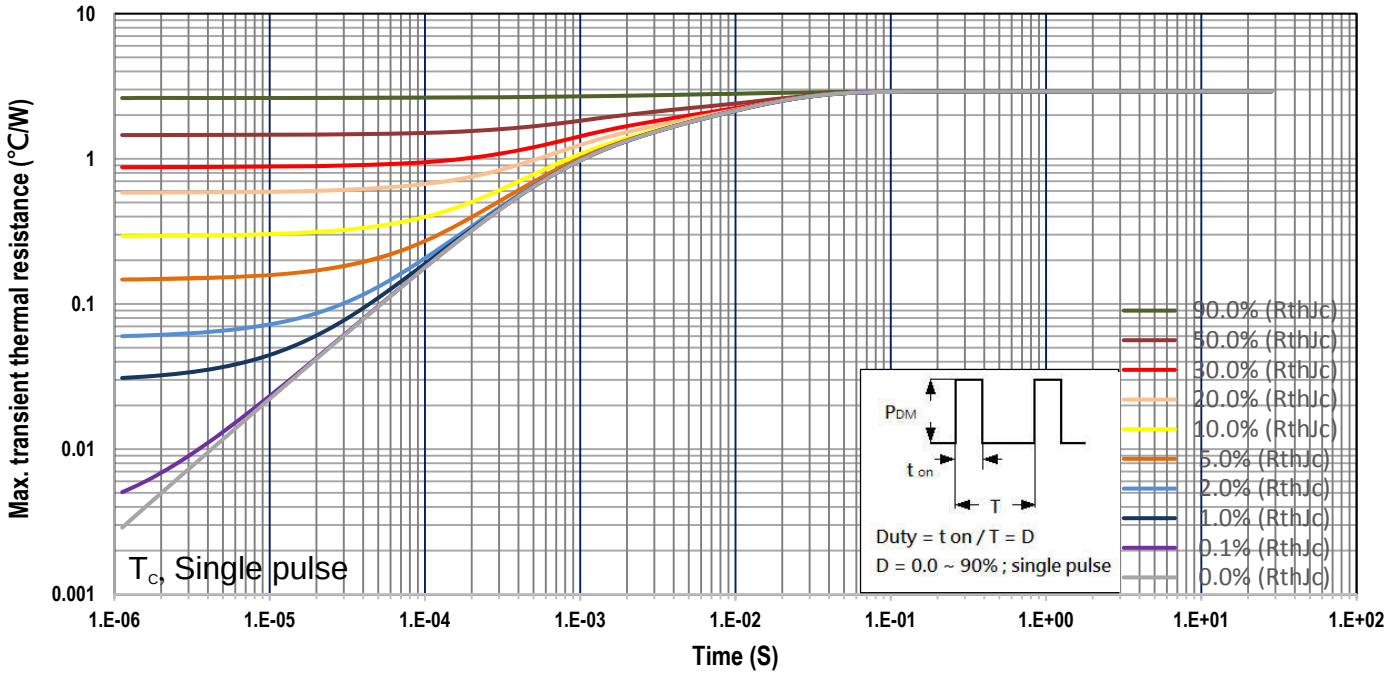


Fig. 14 Transient Thermal Impedance



P-Channel Typical Operating Characteristics

Fig. 15 Output Characteristics

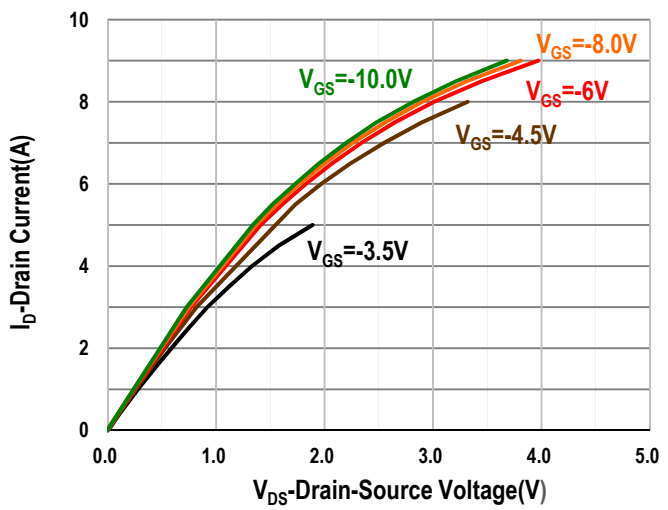


Fig. 16 Gate Threshold Voltage Vs T_a

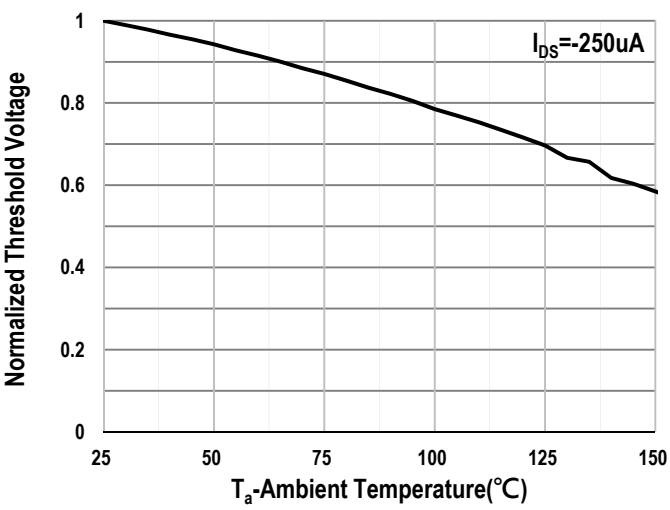


Fig. 17 Drain-Source On Resistance

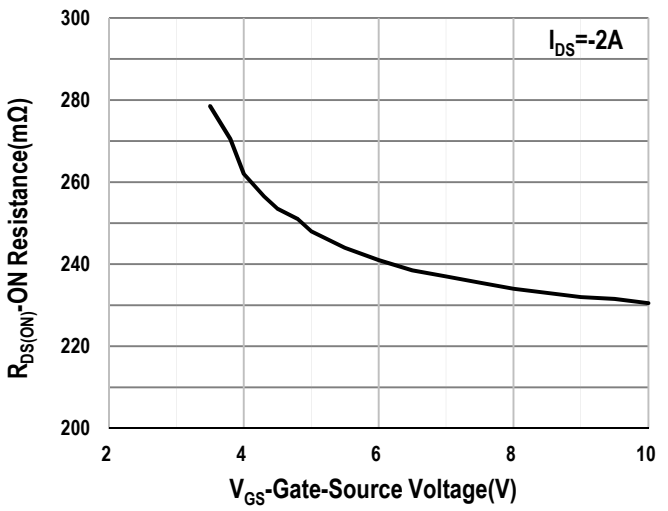


Fig. 18 Normalized On Resistance Vs T_a

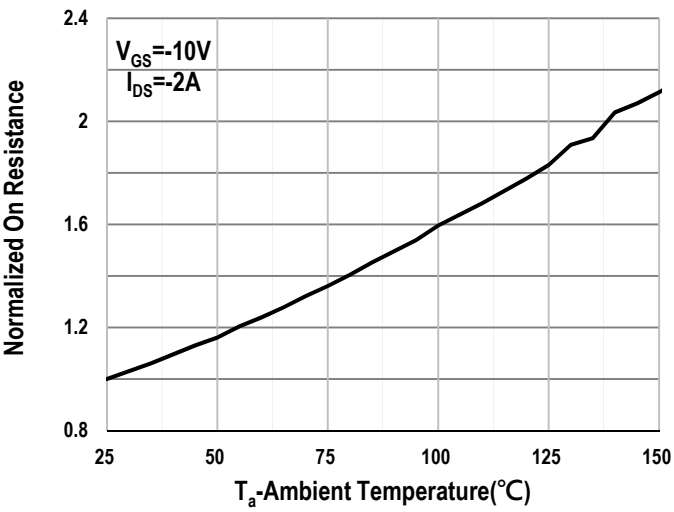


Fig. 19 Drain-Source On Resistance

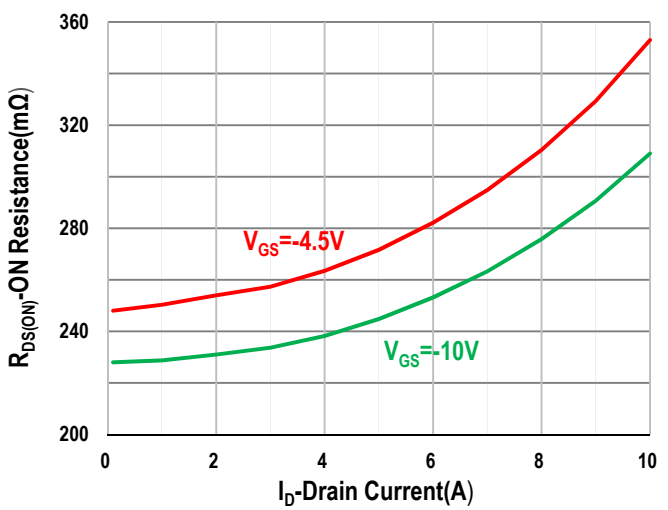
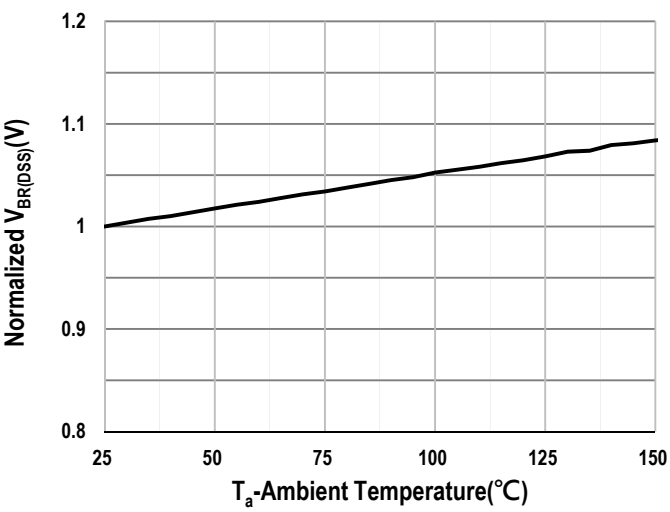


Fig. 20 Drain-source Breakdown Voltage Vs T_A



P-Channel Typical Operating Characteristics

Fig. 21 Capacitance Vs V_{DS}

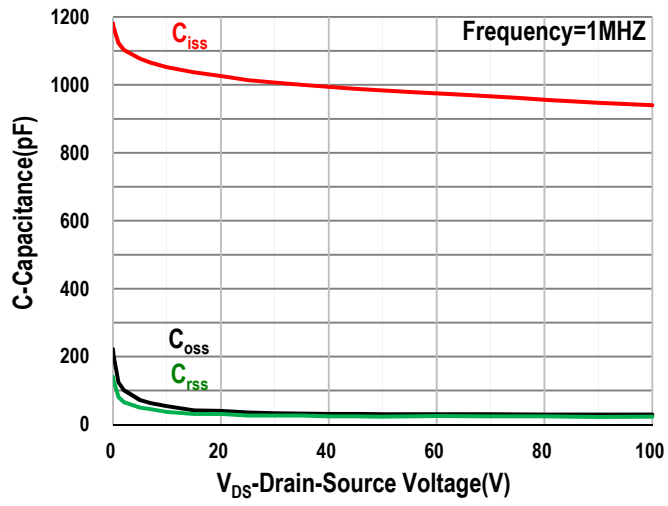


Fig. 22 Gate Charge Vs V_{GS}

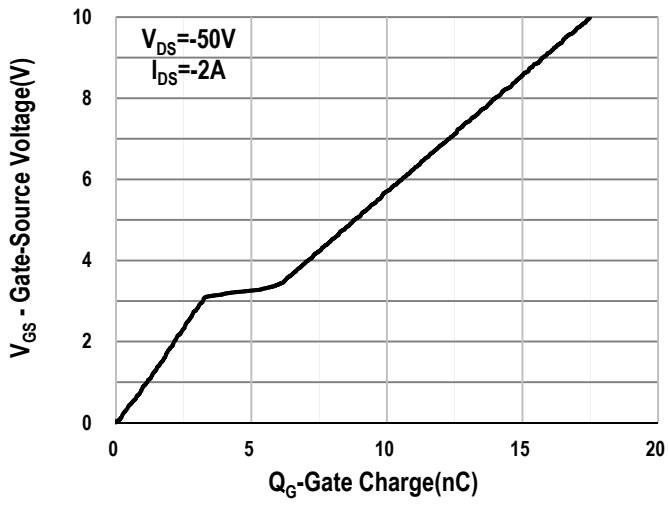


Fig. 23 Power Dissipation Vs Tc

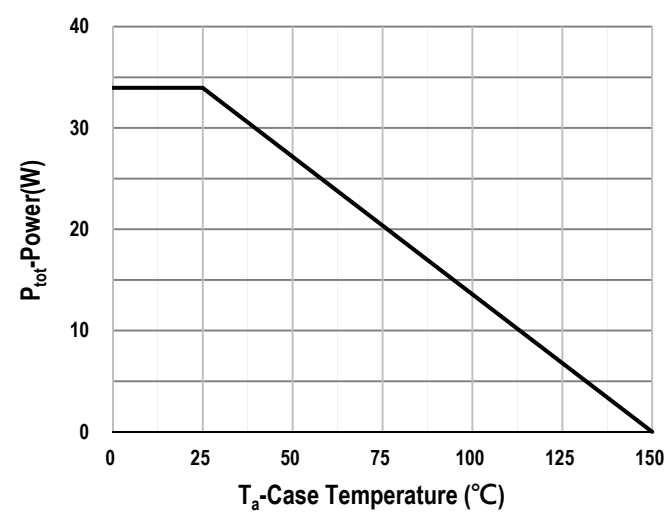


Fig. 24 Drain Current Vs Tc

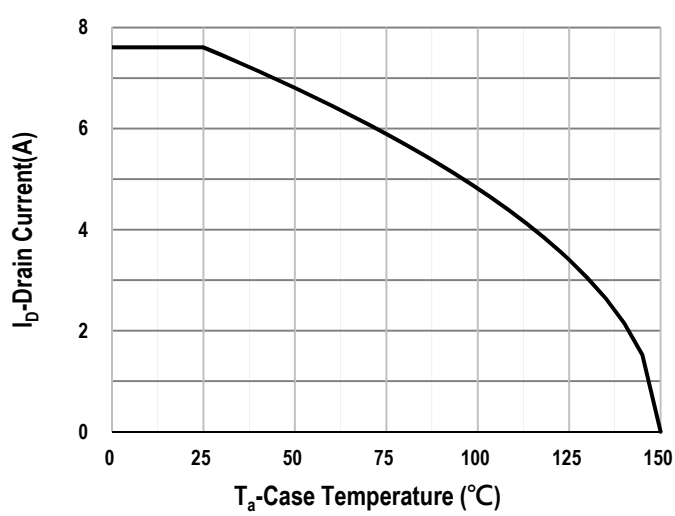


Fig. 25 Body Diode Forward Voltage Vs I_{SD}

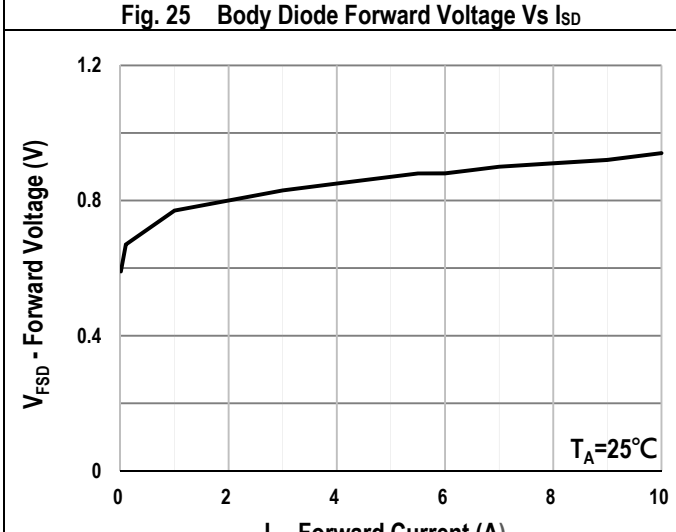


Fig. 26 Body Diode Forward Voltage Vs T_A

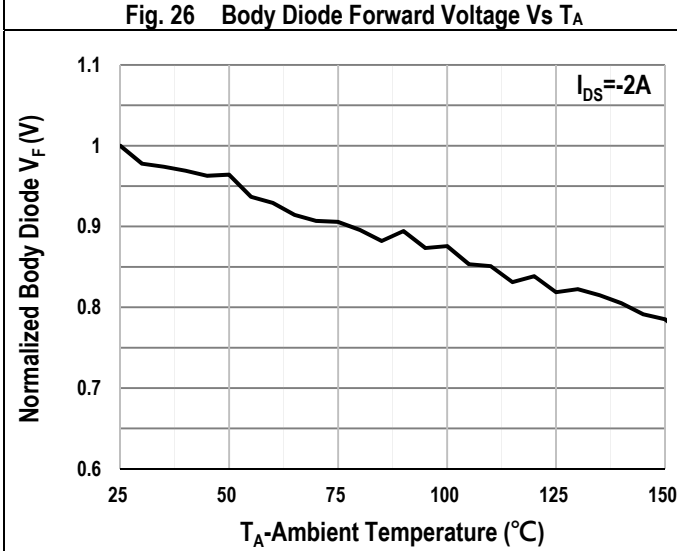


Fig.27 Safe Operation Area

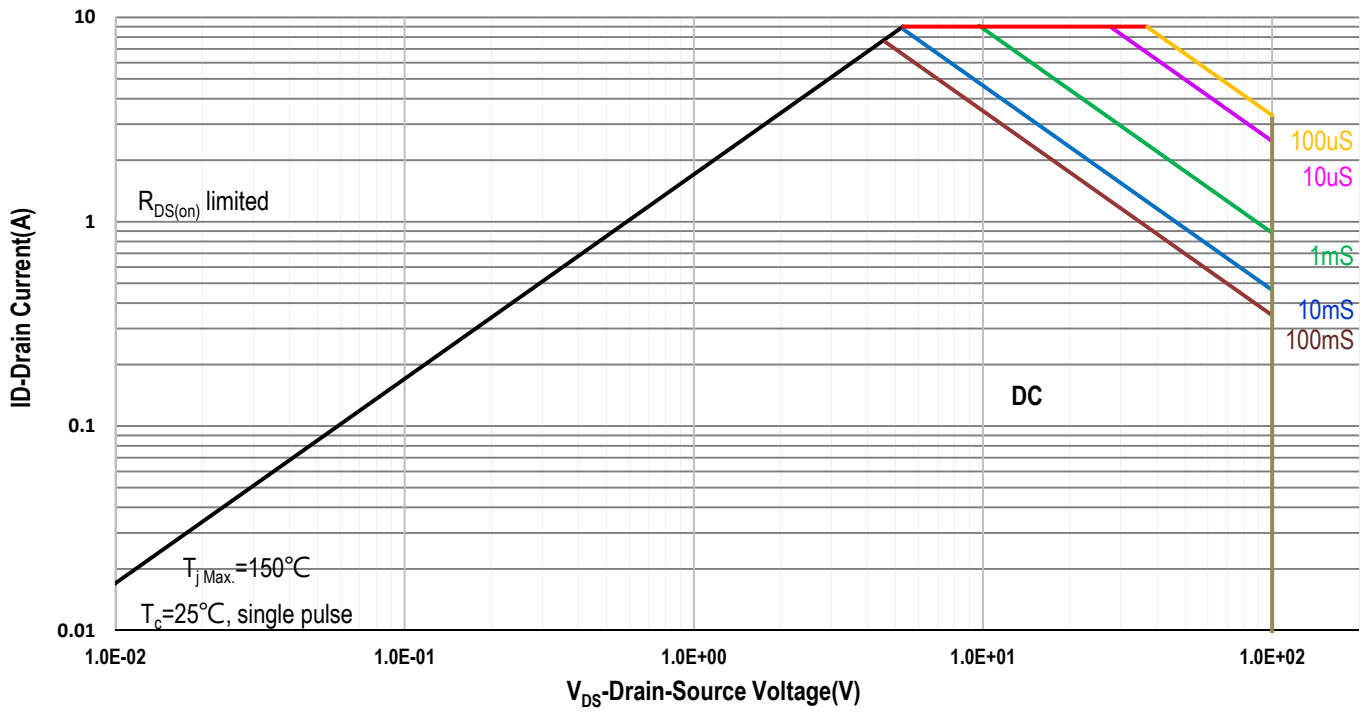
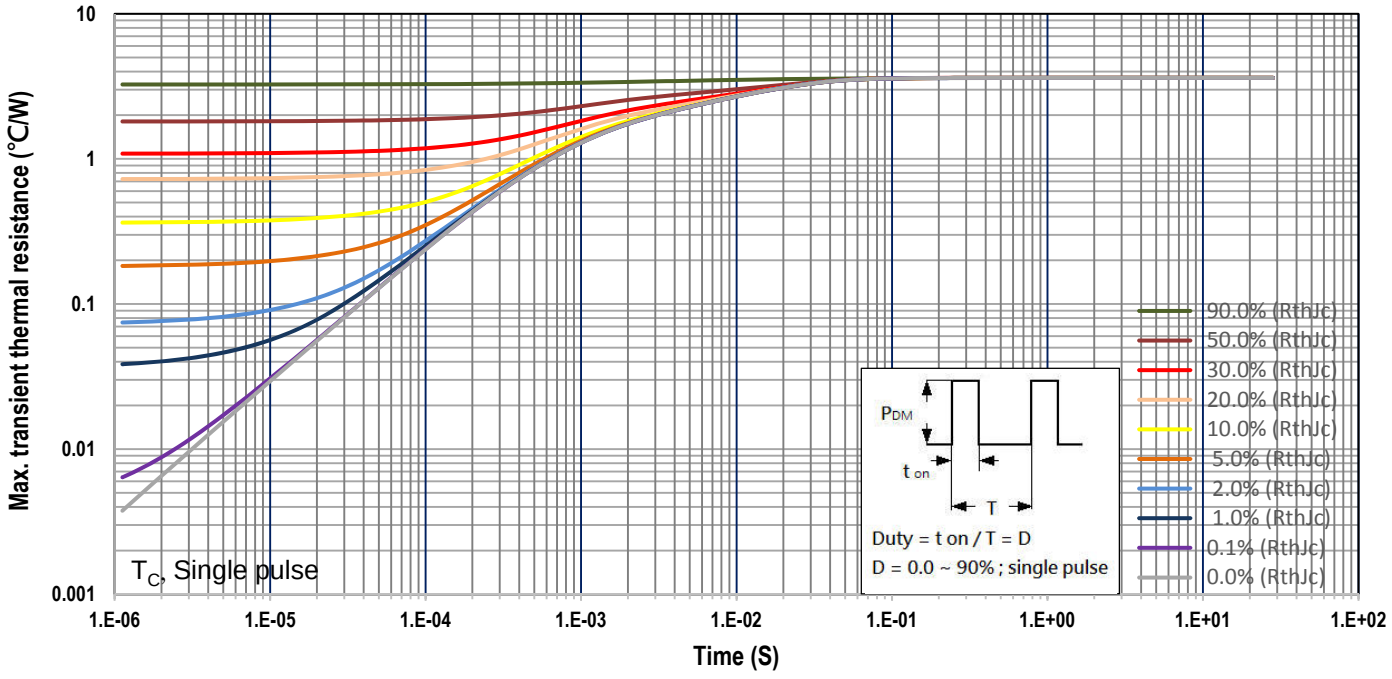
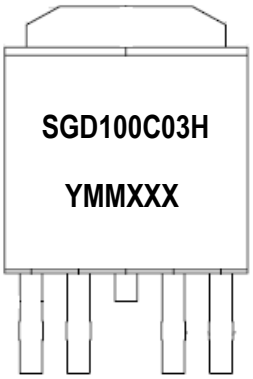


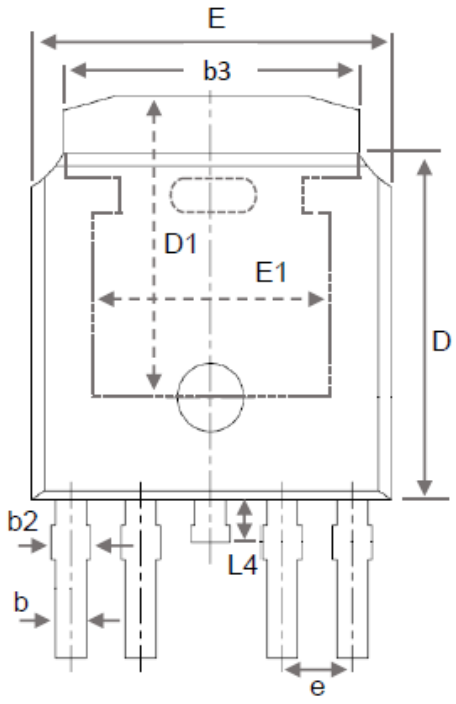
Fig.28 Transient Thermal Impedance

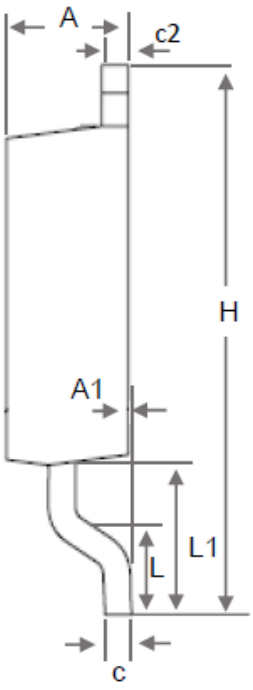


Marking Information

TO-252-4L (H)	Marking Rule
Laser Marking  	Line 1：Device SGD100C03H Line 2：Date Code YMMXXX Y：Year Code MM：Month Code XXX：Serial Number

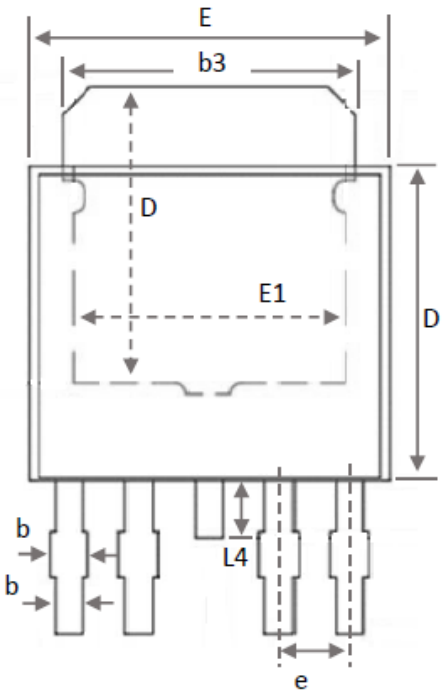
Package of dimension



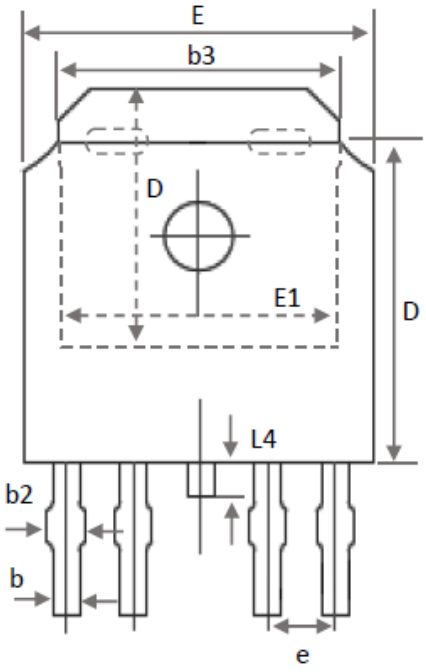


Symbol	Min	Nor	Max
A	2.184	2.292	2.40
A1	-	-	0.25
b	0.40	0.56	0.711
b2	0.45	0.63	0.80
b3	5.10	5.31	5.52
c	0.45	0.53	0.61
c2	0.45	0.53	0.61
D	5.40	5.83	6.25
D1	4.57	-	-
E	6.35	6.58	6.80
E1	3.81	4.61	5.40
e		1.27 Ref.	
H	9.40	9.85	10.30
L	1.397	1.588	1.778
L1	2.40	2.70	3.00
L4	-	-	1.20

SI-TYPE



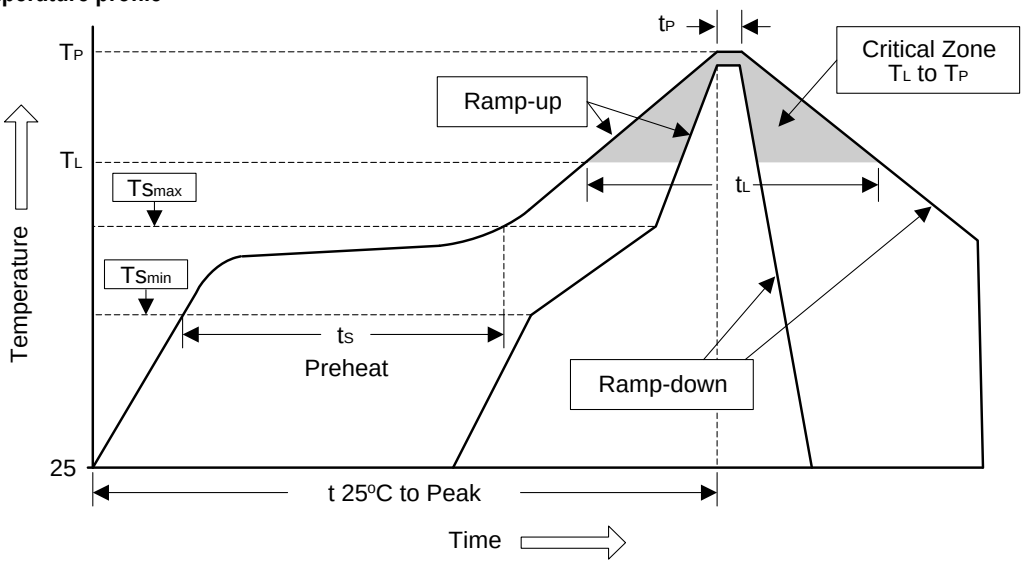
S-Type



Soldering Methods for Silicongear's Products

1. Storage environment: Temperature=10°C to 35°C Humidity=65%±15%
2. Reflow soldering of surface-mount devices

Figure 1: Temperature profile



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	<3°C/sec	<3°C/sec
Preheat - Temperature Min (Ts_{min}) - Temperature Max (Ts_{max}) - Time (min to max) (ts)	 100°C 150°C 60 to 120 sec	 150°C 200°C 60 to 180 sec
Tsmax to T_L - Ramp-up Rate	 <3°C/sec	 <3°C/sec
Time maintained above: - Temperature (T_L) - Time (t_L)	 183°C 60 to 150 sec	 217°C 60 to 150 sec
Peak Temperature (T_P)	240°C +0/-5°C	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10 to 30 sec	20 to 40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25°C to Peak Temperature	<6 minutes	<8 minutes

3. Flow (wave) soldering (solder dipping)

Products	Peak Temperature	Dipping Time
Pb devices.	245°C ±5°C	5sec ±1sec
Pb-Free devices.	260°C +0/-5°C	5sec ±1sec

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