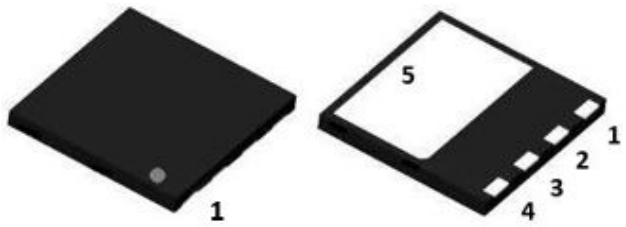
SJ650N180B2

650V N-Channel Enhancement Mode Power MOSFET

Key Electrical Characteristics		
Parameter / Symbol	Value / Description	Unit
$BV_{DSS\ min.}$	650	V
$R_{DS\ (ON)\ Typ.\ @10V}$	148	mΩ
I_D	18.1	A
$V_{TH\ Typ.}$	2.9	V
$Ciss_{\ Typ.}$	1749	pF
$Q_{g\ 10V}$	40.1	nC
ESD (HBM)	≧2	KV

Package Outline

DFN8x8



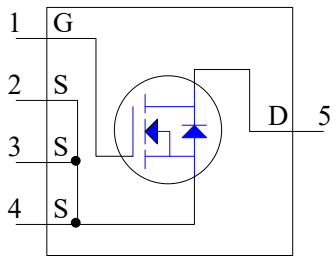
General Description

These devices are N-channel power MOSFET developed using Super Junction structure technology. There is high speed switching capacity, low R_{DSON} parameter, excellent quality and characteristics for these devices. Moreover, it is a good choose in improved efficiency of circuit and raise power density are required. These features combine to be an advantage design for use in wide variety of application including switch mode power design.

Features

- ✧ Fast Switching
- ✧ Low $R_{DS\ (ON)}$ resistance
- ✧ Low Switching Loss
- ✧ Improve ESD protection capabilities
- ✧ More compact and smaller size in package
- ✧ Excellent single pulse avalanche energy
- ✧ Pb-free lead plating and RoHS compliant

Symbol and Pin assignment



Potential Applications

- ◆ Switch Mode Power Supply
- ◆ High efficiency power module
- ◆ LED lighting power system
- ◆ Consumption electronic adaptor or charger
- ◆ Slim and light power circuit

Ordering Information

N.o	Item	Description
01	Orderable P/N	SJ650N180B2
02	Part Number	SJ650N180B2
03	Package Type	DFN8x8
04	Package Code	B
05	Packing Type	Tape & Reel
06	Quantity/pcs	3,000
07	RoHS Status	Halogen-Free

Content

1. Absolute Maximum Ratings (T_J=25°C unless otherwise noted)

Parameter		Symbol	Values			Unit
			Min.	Typ.	Max.	
Drain-Source Voltage		V_{DS}	-	-	650	V
Gate-Source Voltage		V_{GS}	-	-	±30	V
Drain Current-Continuous Note 1	T_C=25°C	I_D	-	-	18.1	A
	T_C=100°C		-	-	11.4	A
Drain Current-Pulsed Note 2	T_C=25°C	I_{DM}	-	-	70	A
Avalanche Current		I_{As}	-	-	6.3	A
Single Pulse Avalanche Energy Note 3		E_{AS}	-	-	158	mJ
Maximum Power Dissipation	T_C=25°C	P_D	-	-	59.2	W
	T_C=100°C		-	-	23.6	W
	Derate Factor Above T_C=25°C		-	-	0.47	W/°C
Body Diode dv/dt Note 4	T_C=25°C, V_{DD}=0~400V	dv/dt	-	-	14.1	V/nS
Max. Operating Junction Temperature		T_J	-	-	150	°C
Storage Temperature Range		T_{STG}	-55	-	150	°C

2. Thermal Resistance Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal resistance, Junction-Case Note 5	$R_{\theta JC}$	Steady State	-	-	2.11	°C/W
Thermal resistance, Junction-Ambient Note 5	$R_{\theta JA}$	Steady State	-	-	64.52	°C/W

Notes:

1. Limited by silicon chip capability and $R_{\theta JC}$ junction-to-case thermal resistance.
2. Must be ensure junction temperature does not exceed 150-degree C. (Pulse Width ≦ 380uS, Duty ≦ 2%)
3. Limited by T_{Jmax}, starting T_J=25°C, L=8 mH, R_g=25Ω, I_{AS}=6.3A, V_{GS}=10V.
4. V_{DD} = 0~400 V, I_{SD}=I_S ≦ 10 A starting T_C = 25°C
5. The value of thermal resistance is measured with the single device put on cooling plate under a still air environment temperature is 25 degree C based on JEDEC standard JESD51-14 and JESD51-2a. Thermal resistance obtained depends on the user's specific board design and given application.
6. $C_{o(er)}$ is fixed capacitance that gives same stored energy as C_{OSS} while V_{DS} rising to 400V from 0V.
7. $C_{o(tr)}$ is fixed capacitance that gives same charging time as C_{OSS} while V_{DS} rising to 400V from 0V.

3. Electrical Characteristics (T_J=25°C unless otherwise noted)

STATIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_{DS}=250μA	650	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	-	-	1	uA
		V_{DS}=650V, V_{GS}=0V, T_J=125°C	-	-	10	uA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	-	-	±100	nA

STATIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_{DS}=250μA	2.7	2.9	3.3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_{DS}=12A	-	148	180	mΩ
Gate Resistance	R_G	VGS=0V, VDS=0V, f=1MHz	-	4.7	-	Ω
Forward Transconductance	gfs	VDS=10V, IDS=12A	-	15.1	-	S

DYNAMIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Input Capacitance	C_{iss}	V_{DD}=650V, V_{DS}=325V, V_{GS}=0V, F=1MHz	-	1749	-	pF
Output Capacitance	C_{oss}	V_{DD}=650V, V_{DS}=325V, V_{GS}=0V, F=1MHz	-	42.2	-	pF
Reverse Transfer Capacitance	C_{rss}	V_{DD}=650V, V_{DS}=325V, V_{GS}=0V, F=1MHz	-	5.6	-	pF
Effective output capacitance-energy	$C_{o(er)}$	V_{DD}=400V, V_G=10V, energy related Note 6	-	145	-	pF
Effective output capacitance-time	$C_{o(tr)}$	V_{DD}=400V, V_G=10V, time related Note 7	-	603	-	pF
Turn-On Delay Time	$T_{d(on)}$	V_{DS}=400V, V_{GS}=10V, I_{DS}=10A, R_{GEN}=10Ω	-	18	-	nS
Rise Time	t_r	V_{DS}=400V, V_{GS}=10V, I_{DS}=10A, R_{GEN}=10Ω	-	22.6	-	nS
Turn-Off Delay Time	$T_{d(off)}$	V_{DS}=400V, V_{GS}=10V, I_{DS}=10A, R_{GEN}=10Ω	-	87.5	-	nS
Fall Time	t_f	V_{DS}=400V, V_{GS}=10V, I_{DS}=10A, R_{GEN}=10Ω	-	33.5	-	nS

GATE CHARGE CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Gate charge total	$Q_{g\ 10V}$	V_{DD}=400V, I_D=10A, V_{GS}=0 to 10V	-	40.1	-	nC
Gate to Source Gate Charge	Q_{gs}	V_{DD}=400V, I_D=10A, V_{GS}=0 to 10V	-	9.6	-	nC
Gate to Drain Charge	Q_{gd}	V_{DD}=400V, I_D=10A, V_{GS}=0 to 10V	-	12.8	-	nC
Gate plateau voltage	$V_{plateau}$	V_{DD}=400V, I_D=10A, V_{GS}=0 to 10V	-	4.9	-	V

BODY DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Diode continuous forward current	I_S	T_C=25°C	-	-	18.1	A
Diode pulsed forward current	I_{SM}	T_C=25°C	-	-	70	A
Diode forward Voltage	V_{SD}	T_C=25°C, V_{GS}=0V, I_S= 12A	-	0.86	1.0	V
Diode reverse Recovery Time	t_{rr}	V_{DD}=400V, I_{SD}=10A, T_C=25°C, di/dt=50A/μs	-	332	-	nS
Diode reverse Recovery Charge	Q_{rr}	V_{DD}=400V, I_{SD}=10A, T_C=25°C, di/dt=50A/μs	-	3086	-	nC
Diode peak reverse recovery current	I_{rm}	V_{DD}=400V, I_{SD}=10A, T_C=25°C, di/dt=50A/μs	-	20.3	-	A

4. Typical Operating Characteristics diagrams

Fig. 1: Output Characteristics

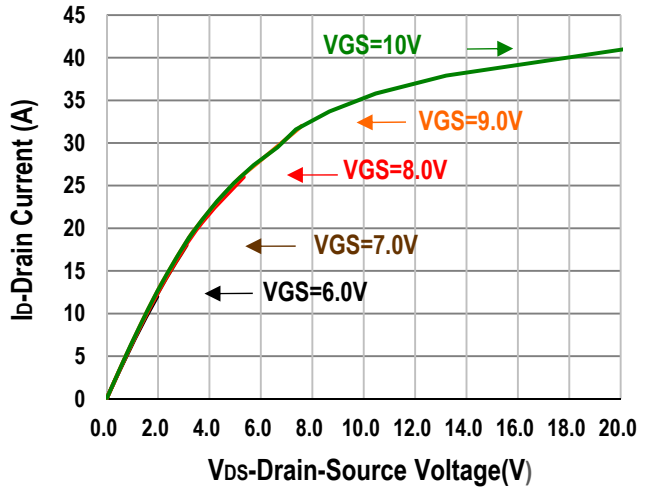


Fig. 2: Normalized $V_{(TH)GS}$ Voltage Vs. T_A

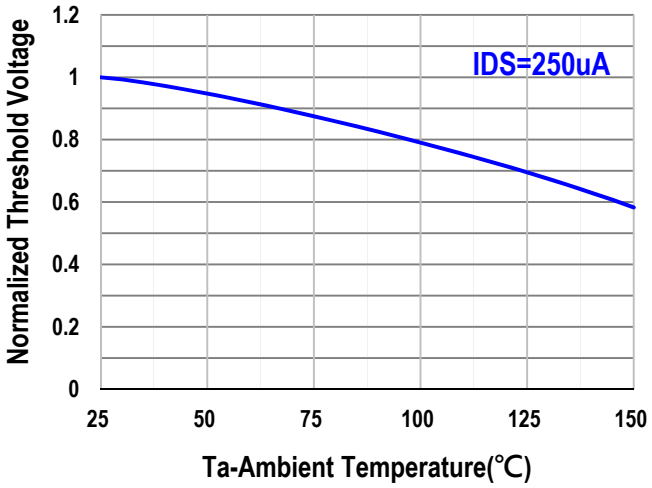


Fig. 3: Drain-Source On Resistance Vs V_{GS}

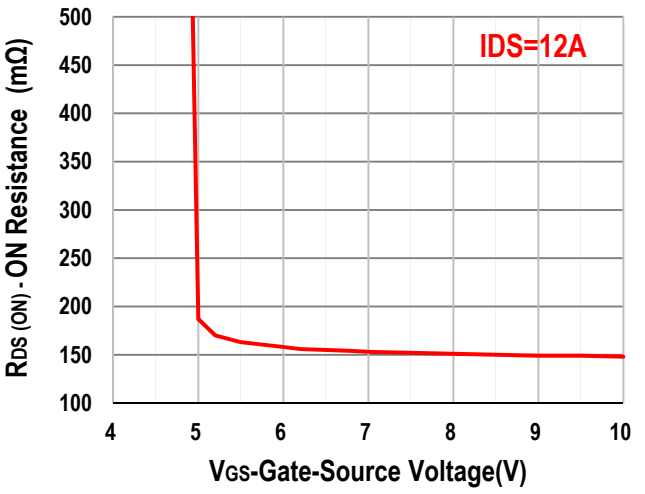


Fig. 4: Normalized $R_{DS(ON)}$ Resistance Vs. T_A

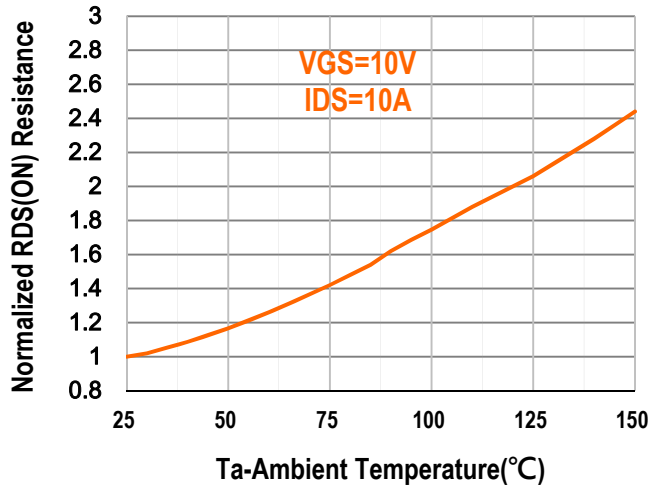


Fig. 5: Drain-Source On Resistance Vs I_D

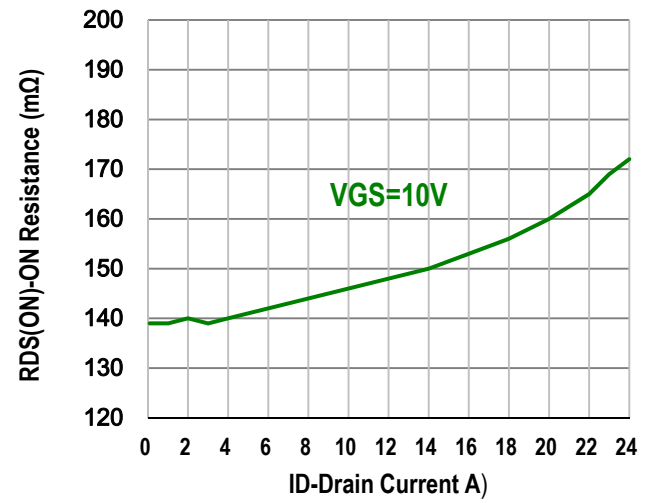
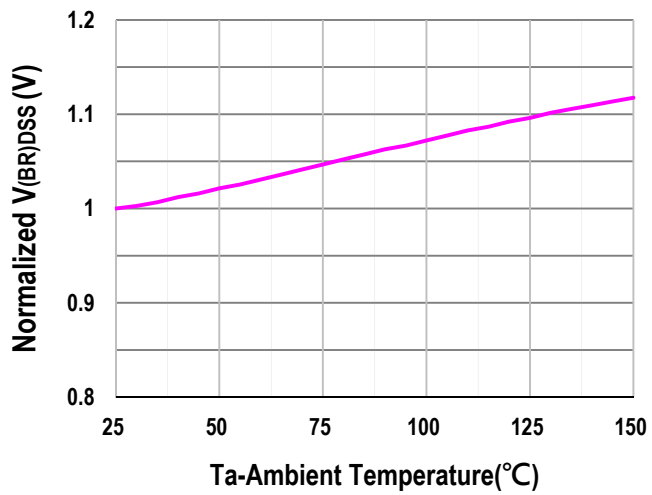


Fig. 6: Normalized BVDSS Voltage Vs TA



4. Typical Operating Characteristics diagrams

Fig. 7: Typical Capacitance Variation Vs V_{DS}

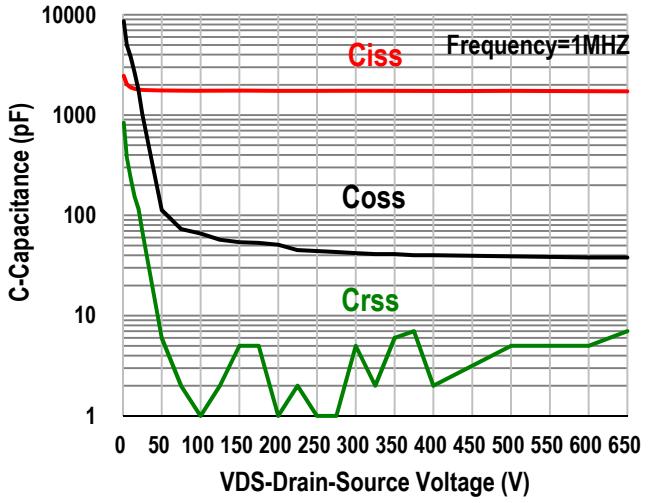


Fig. 8: Gate Charge Vs V_{GS}

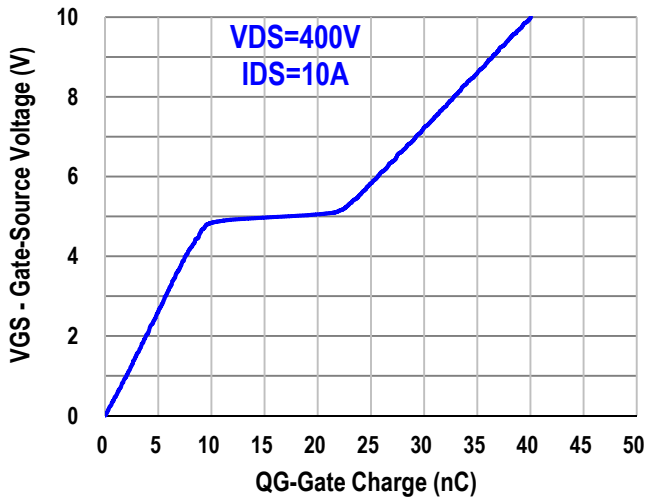


Fig. 9: Power Dissipation Vs. T_C

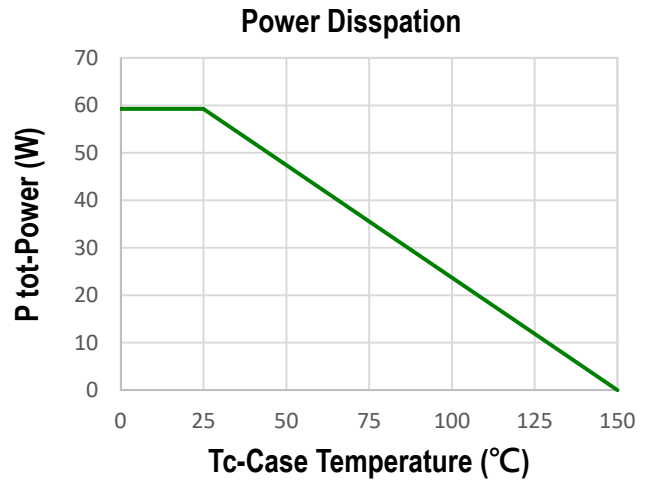


Fig. 10: Drain Current Vs. T_C

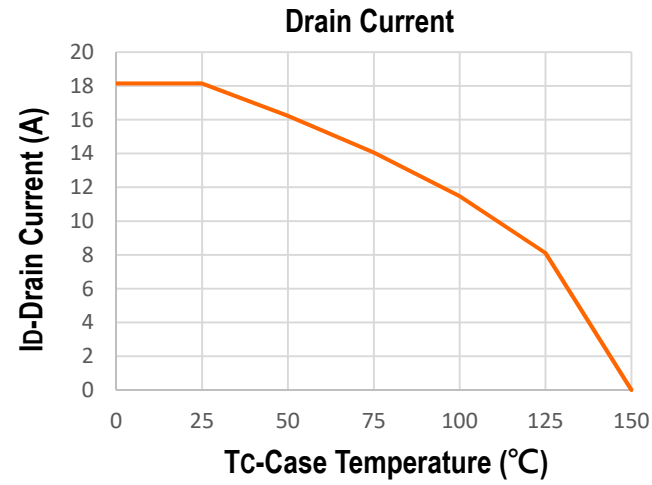


Fig. 11: Body Diode Forward Voltage Vs. I_S

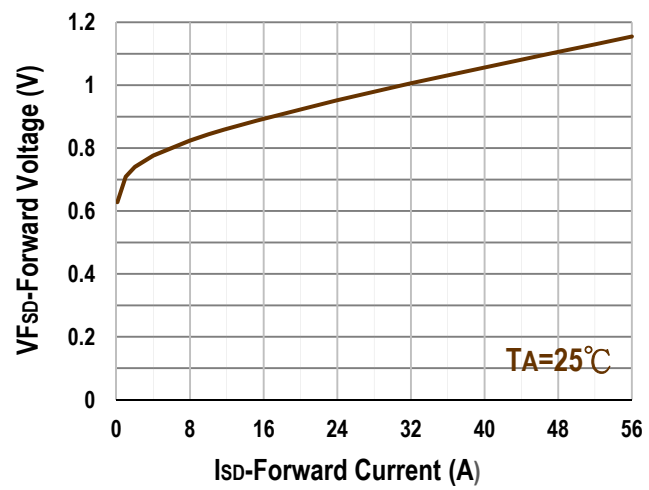
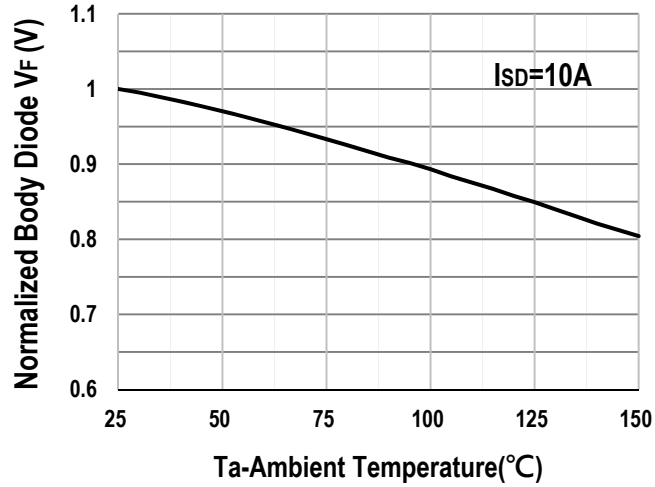


Fig. 12: Body Diode Forward Voltage Vs. T_A



4. Typical Operating Characteristics diagrams

Fig. 13: Safe Operation Area

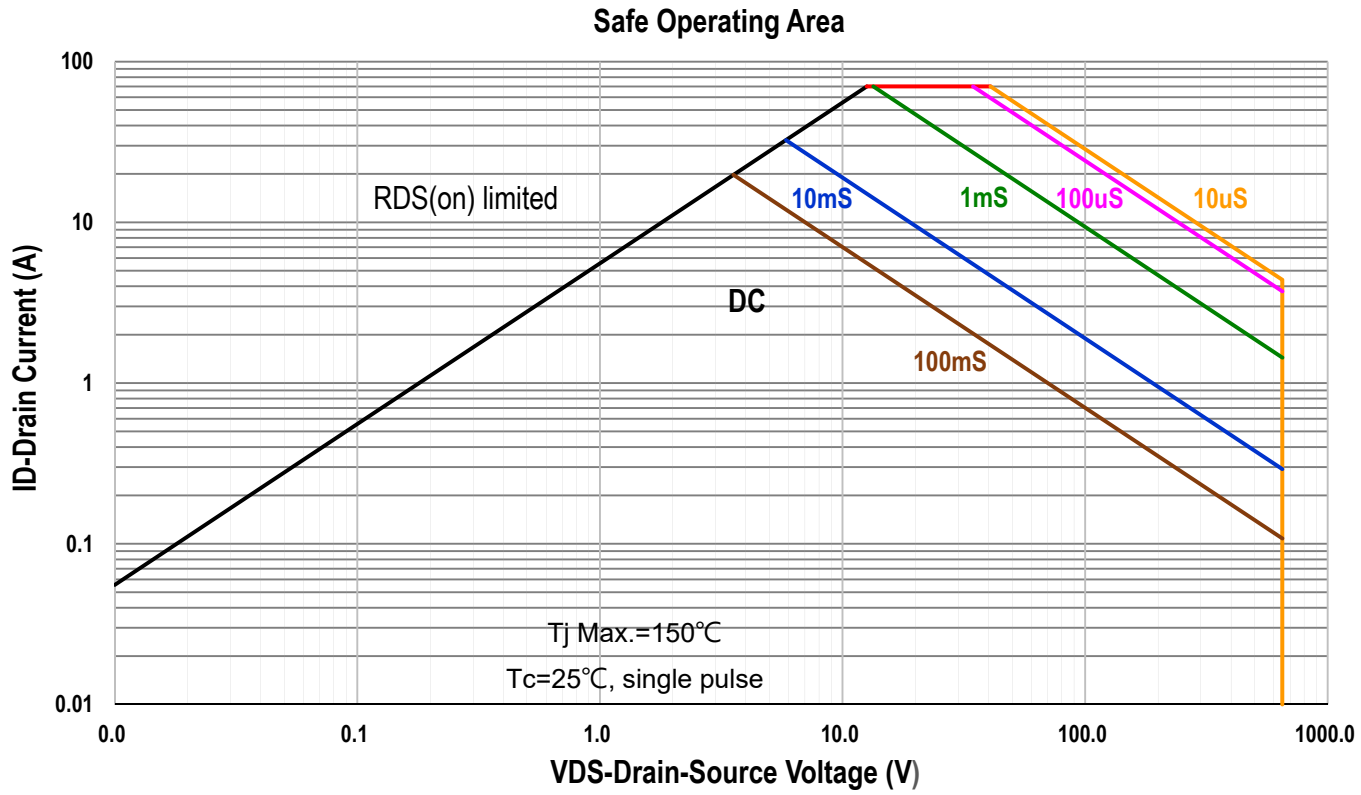
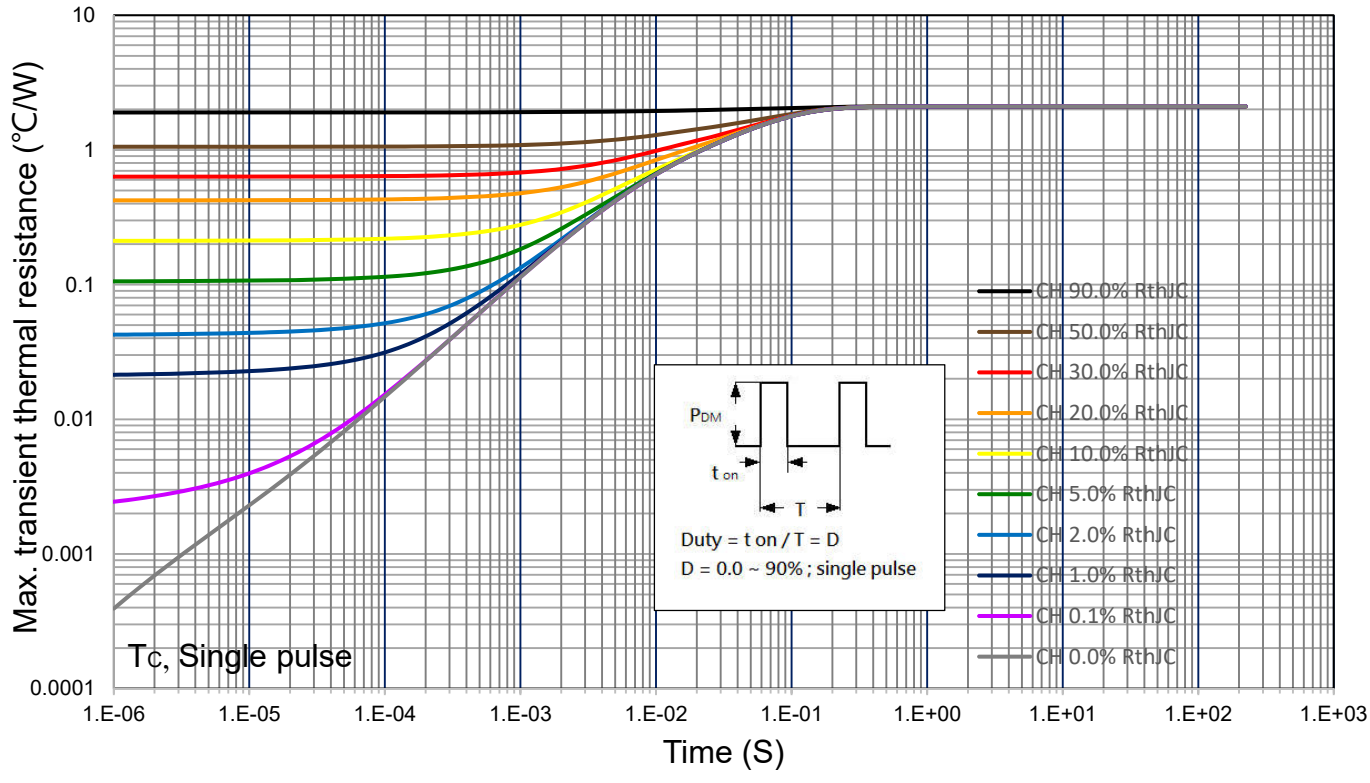


Fig. 14: Transient Thermal Impedance



5. Measurement Schematic

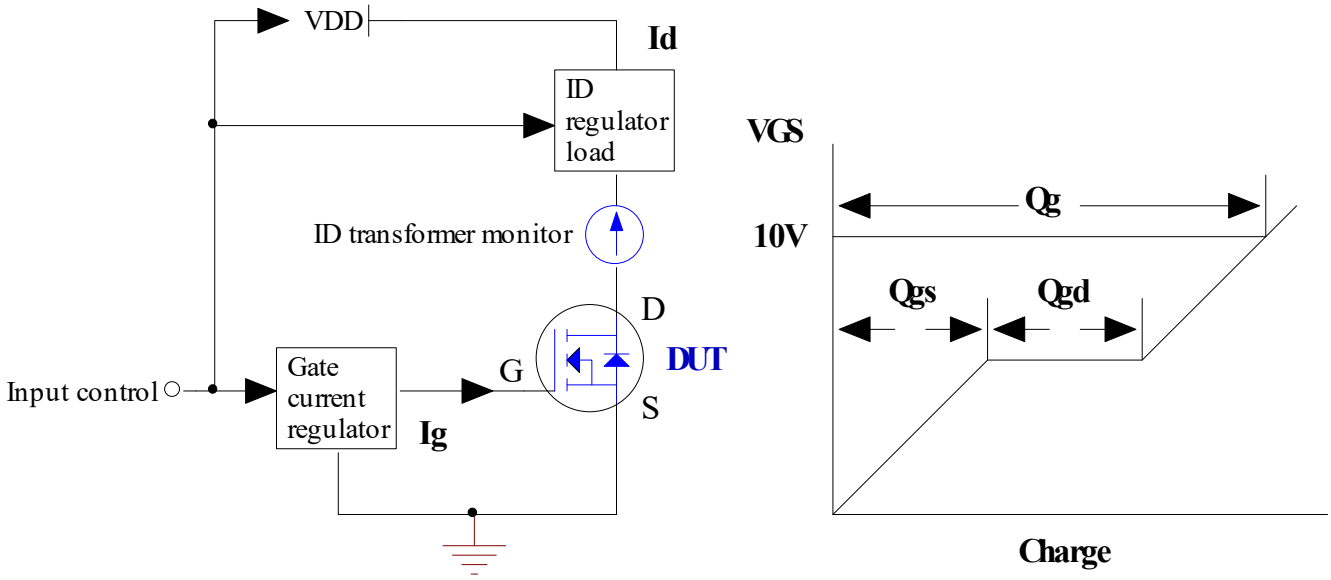


Diagram 5.1 Gate Charge Measurement Circuit and Waveforms

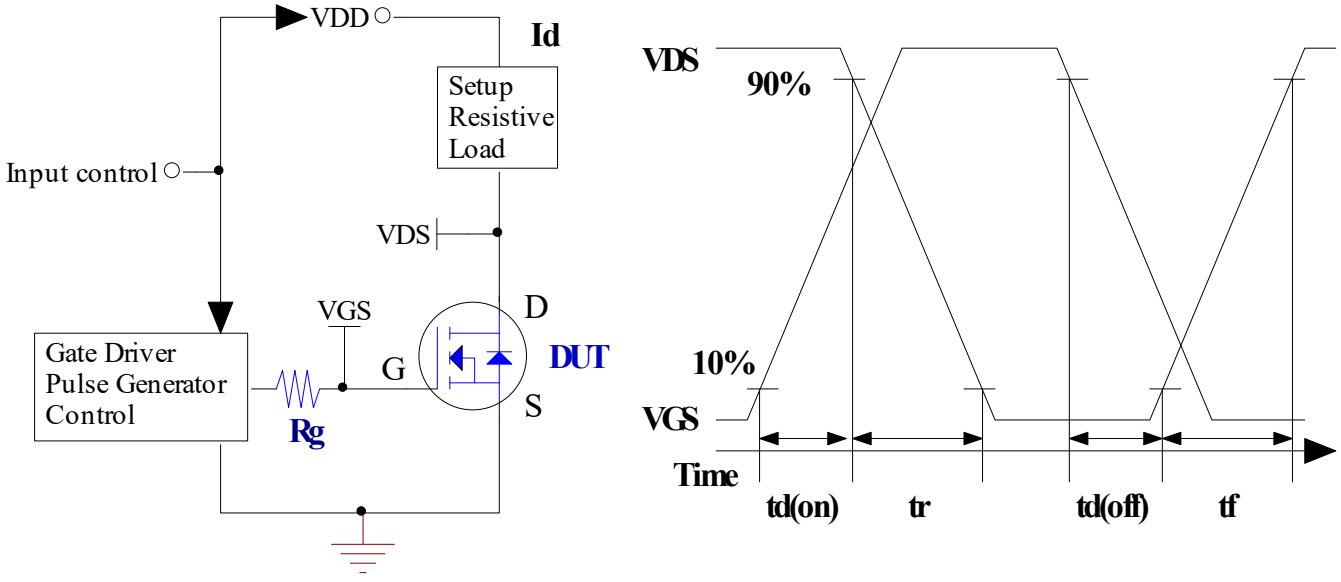


Diagram 5.2 Resistive Switching Measurement Circuit and Waveforms

5. Measurement Schematic

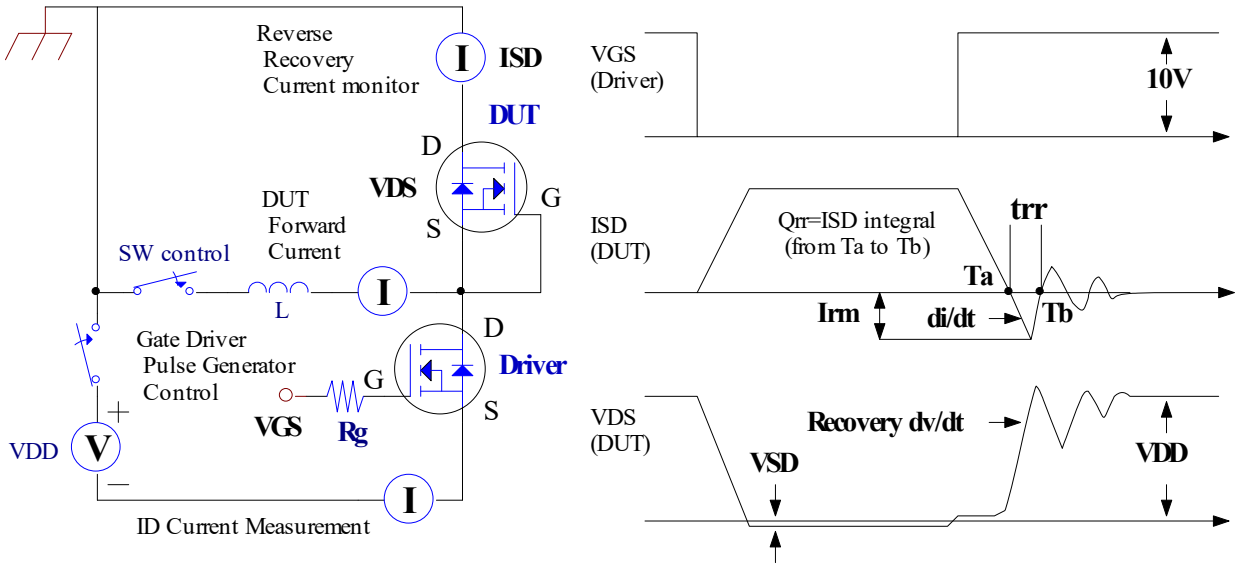


Diagram 5.3 Body Diode Recovery Characteristics Measurement Circuit and Waveforms

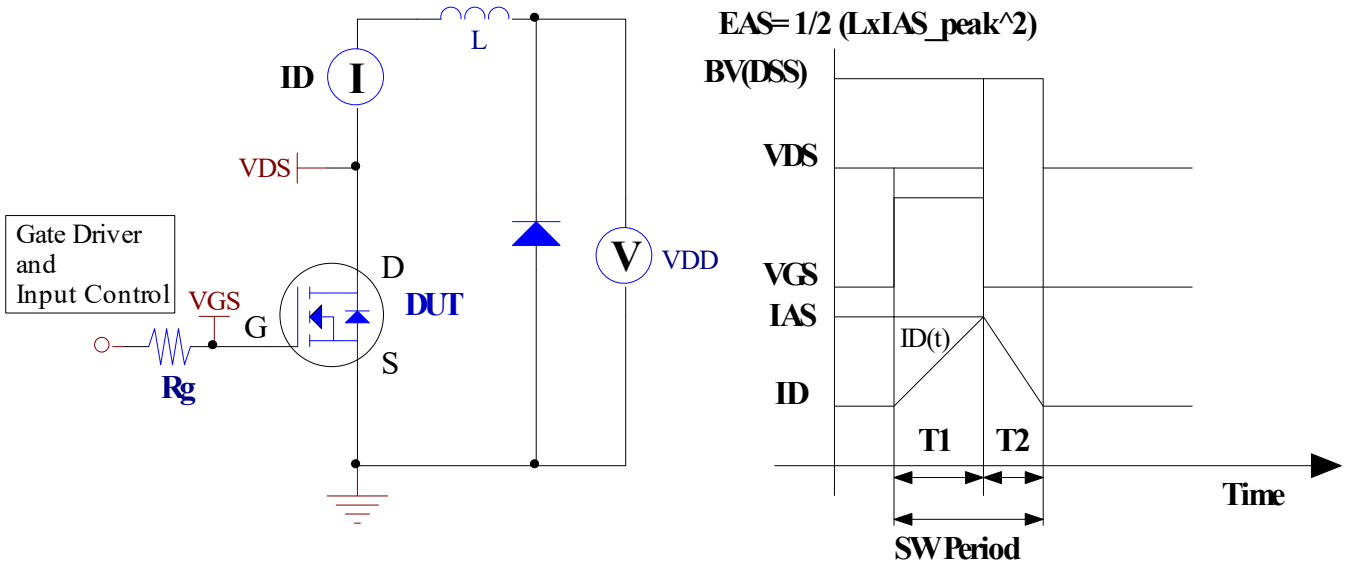
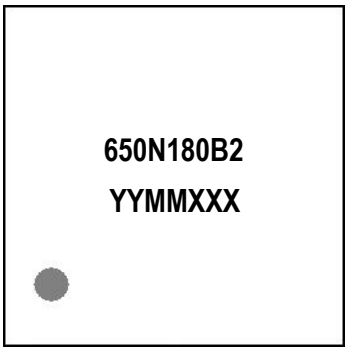


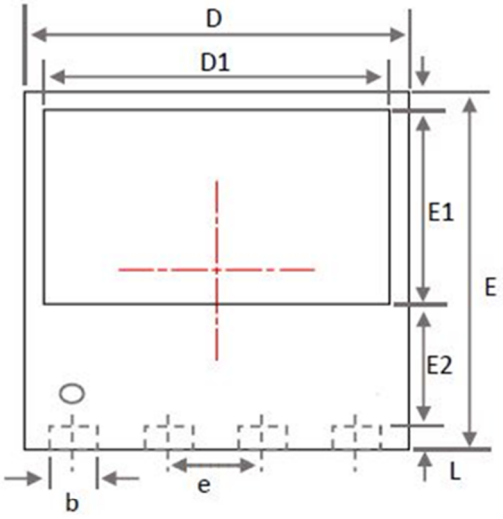
Diagram 5.4 Unclamped Inductive Switching Measurement Circuit and Waveforms

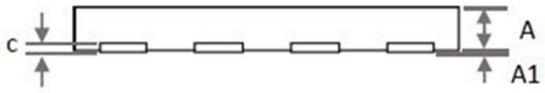
6. Marking Information

DFN8x8 (B)	Marking Rule
Laser Marking  	Line 1：Device 650N180B2 Line 2：Date Code YYMMXXX YY：Year Code MM：Month Code XXX：Serial Number

7. Package of Dimension

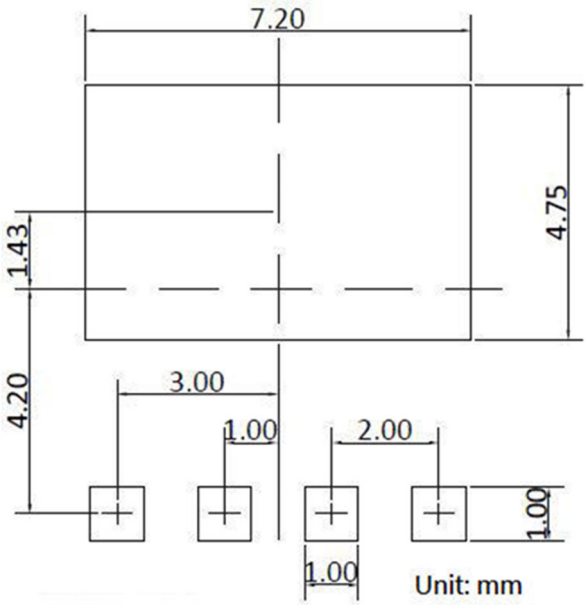
Package type: DFN8x8





Symbol	Min	Nor	Max
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.90	1.00	1.10
c	0.10	0.20	0.30
D	7.90	8.00	8.10
D1	7.10	7.20	7.30
E	7.90	8.00	8.10
E1	4.25	4.35	4.45
E2	2.65	2.75	2.85
E3	0.30	0.40	0.50
e	2.00	2.00	2.00
L	0.40	0.50	0.60

8. Land pattern (Footprint)



Note 1: Land pattern (Footprint) design is for reference only.
Note 2: Package body sizes exclude mold flash and burrs.
Note 3: Dimension is measured in gauge plane.
Note 4: Tolerance 0.1mm unless otherwise specified.

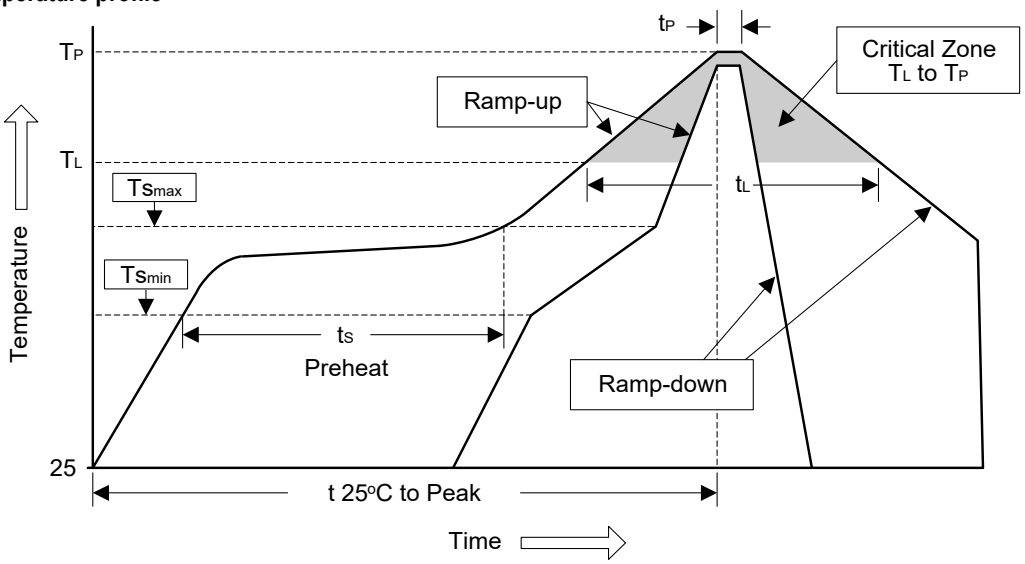
9. Appendix

Appendix-A

Soldering Methods for Silicongear's Products (Just for SMD type of device)

1. Storage environment: Temperature=10°C to 35°C Humidity=65%±15%
2. Reflow soldering of surface-mount devices

Figure 1: Temperature profile



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	<3°C/sec	<3°C/sec
Preheat - Temperature Min (Ts_{min}) - Temperature Max (Ts_{max}) - Time (min to max) (ts)	 100°C 150°C 60 to 120 sec	 150°C 200°C 60 to 180 sec
Tsmax to T_L - Ramp-up Rate	 <3°C/sec	 <3°C/sec
Time maintained above: - Temperature (T_L) - Time (t_L)	 183°C 60 to 150 sec	 217°C 60 to 150 sec
Peak Temperature (T_P)	240°C +0/-5°C	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10 to 30 sec	20 to 40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25°C to Peak Temperature	<6 minutes	<8 minutes

3. Flow (wave) soldering (solder dipping)

Products	Peak Temperature	Dipping Time
Pb devices.	245°C ±5°C	5sec ±1sec
Pb-Free devices.	260°C +0/-5°C	5sec ±1sec

9. Appendix

Appendix-B

Important Notice