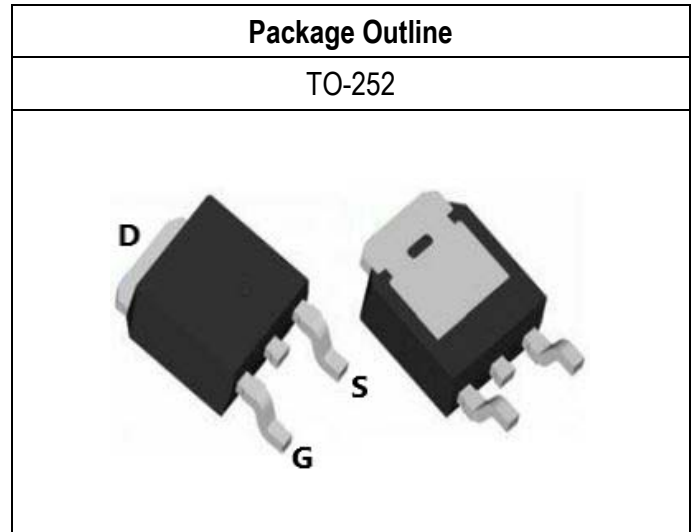


Key Electrical Characteristics		
Parameter / Symbol	Value / Description	Unit
$BV_{DSS \text{ min.}}$	650	V
$R_{DS(ON) \text{ Typ. @10V}}$	0.35	Ω
I_D	10	A
$V_{TH \text{ Typ.}}$	3.0	V
$C_{iss \text{ Typ.}}$	732	pF
$Q_g \text{ 10V}$	17.6	nC
E_{AS}	43	mJ



General Description

These devices are N-channel power MOSFET developed using Super Junction structure technology. There is high speed switching capacity, low $R_{DS(on)}$ parameter, excellent quality and characteristics for these devices. Moreover, it is a good choose in improved efficiency of circuit and raise power density are required. These features combine to be an advantage design for use in wide variety of application including switch mode power design.

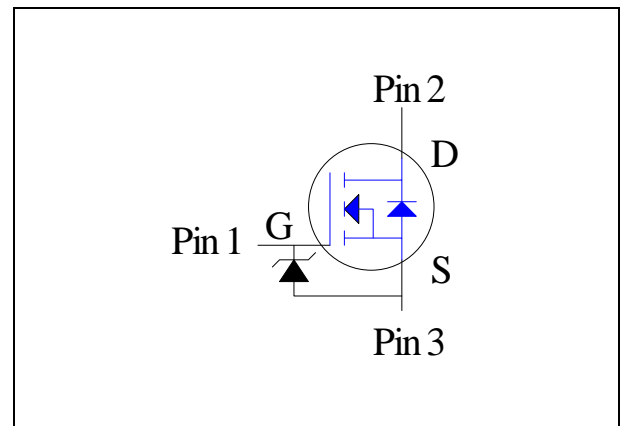
Features

- ✧ Fast Switching
- ✧ Low $R_{DS(on)}$ Resistance
- ✧ Low Gate Charge
- ✧ Low Switching Loss
- ✧ Integrated ESD Protection Diode
- ✧ 100% Single Pulse Avalanche Energy Test
- ✧ Pb-free lead plating and RoHS compliant

Potential Applications

- ◆ AC to DC Converter
- ◆ Electronic Ballasts and LED lighting power
- ◆ Consumer electronics Adaptor or Charger
- ◆ Network equipment and Display power supply unit
- ◆ Switch Mode Power Supply

Symbol and Pin assignment



Ordering Information

Item	Description
Orderable P/N	SJ650N380D2
Package Type	TO-252
Package Code	D
Packing Type	Tape & Reel
Quantity/pcs	2,500
RoHS Status	Halogen-Free

Content

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1. Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Values			Unit	
		Min.	Typ.	Max.		
Drain-Source Voltage	V_{DS}	-	-	650	V	
Gate-Source Voltage	V_{GS}	-	-	± 30	V	
Drain Current-Continuous ^{Note 1}	I_D	$T_C=25^\circ\text{C}$	-	-	10	A
		$T_C=100^\circ\text{C}$	-	-	6.0	A
Drain Current-Pulsed ^{Note 2}	I_{DM}	-	-	18	A	
Avalanche Current	I_{AS}	-	-	3.3	A	
Single Pulse Avalanche Energy ^{Note 3}	E_{AS}	-	-	43	mJ	
Maximum Power Dissipation	P_D	$T_C=25^\circ\text{C}$	-	-	87	W
		$T_C=100^\circ\text{C}$	-	-	35	W
		Derate Factor Above $T_C=25^\circ\text{C}$	-	-	0.69	W/ $^\circ\text{C}$
Body Diode dv/dt ^{Note 4}	dv/dt	-	-	1.5	V/nS	
Max. Operating Junction Temperature	T_J	-	-	150	$^\circ\text{C}$	
Storage Temperature Range	T_{STG}	-55	-	150	$^\circ\text{C}$	

2. Thermal Resistance Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal resistance, Junction-Case ^{Note 5}	$R_{\theta JC}$	Steady State	-	-	1.43	$^\circ\text{C}/\text{W}$
Thermal resistance, Junction-Ambient ^{Note 5}	$R_{\theta JA}$	Steady State	-	-	58.72	$^\circ\text{C}/\text{W}$

Notes:

- Limited by silicon chip capability and $R_{\theta JC}$ junction-to-case thermal resistance.
- Must be ensure junction temperature does not exceed 150-degree C. (Pulse Width $\leq 380\mu\text{s}$, Duty $\leq 2\%$)
- Limited by T_{Jmax} , starting $T_J=25^\circ\text{C}$, $L=8\text{ mH}$, $R_g=25\Omega$, $I_{AS}=3.3\text{A}$, $V_{GS}=10\text{V}$.
- $V_{DD} = 0\sim 100\text{ V}$, $I_{SD}=I_S \leq 6\text{ A}$ starting $T_C = 25^\circ\text{C}$
- The value of thermal resistance is measured with the single device put on cooling plate under a still air environment temperature is 25 degree C based on JEDEC standard JESD51-14 and JESD51-2a. Thermal resistance obtained depends on the user's specific board design and given application.
- $C_{o(er)}$ is fixed capacitance that gives same stored energy as C_{OSS} while V_{DS} rising to 400V from 0V.
- $C_{o(tr)}$ is fixed capacitance that gives same charging time as C_{OSS} while V_{DS} rising to 400V from 0V.

3. Electrical Characteristics (T_J=25°C unless otherwise noted)

STATIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _{DS} =250μA	650	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =650V, V _{GS} =0V	-	-	1	μA
		V _{DS} =650V, V _{GS} =0V, T _J =125°C	-	-	10	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	-	-	±1	μA

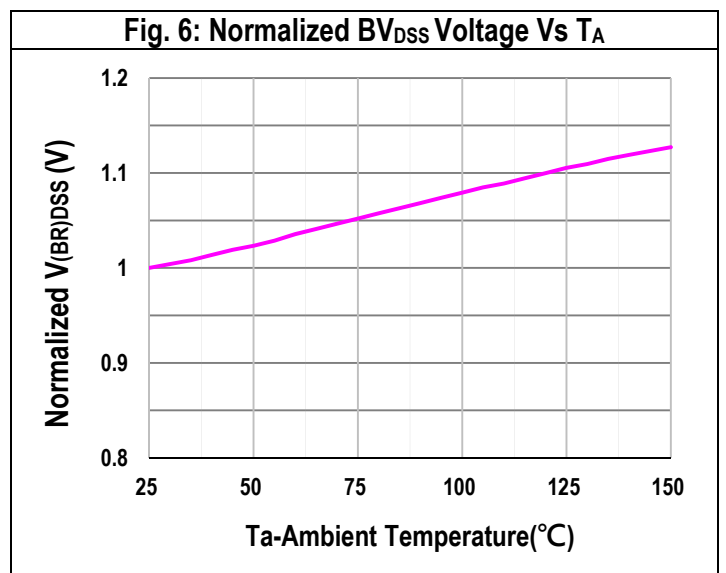
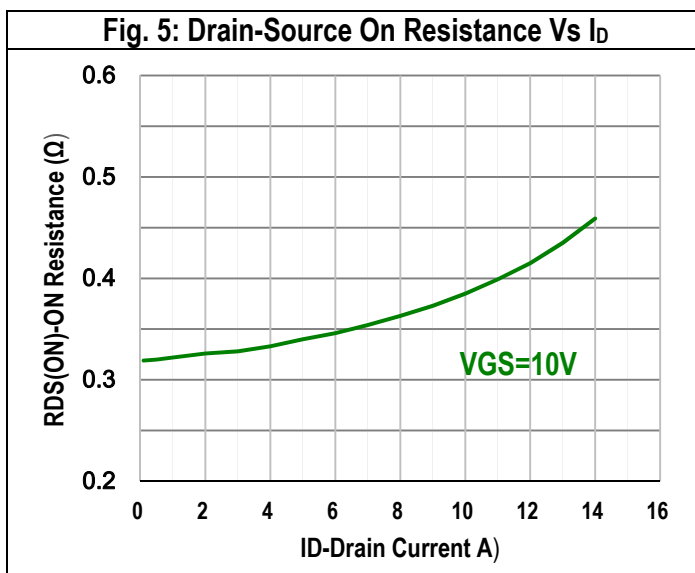
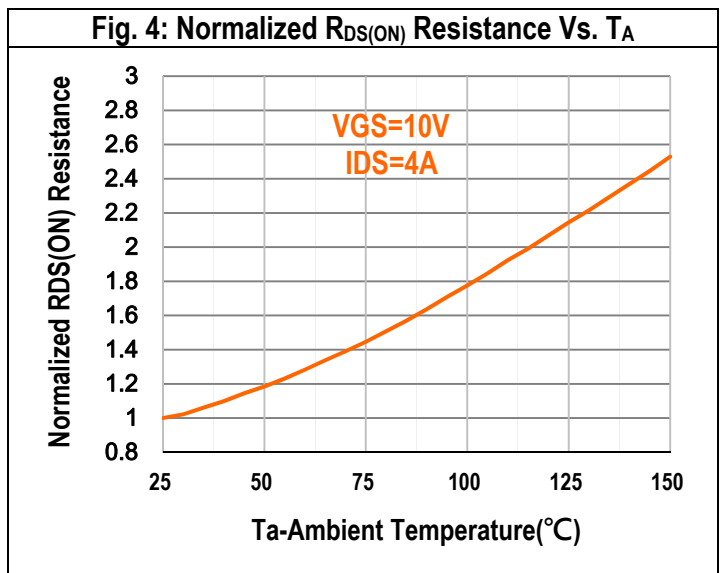
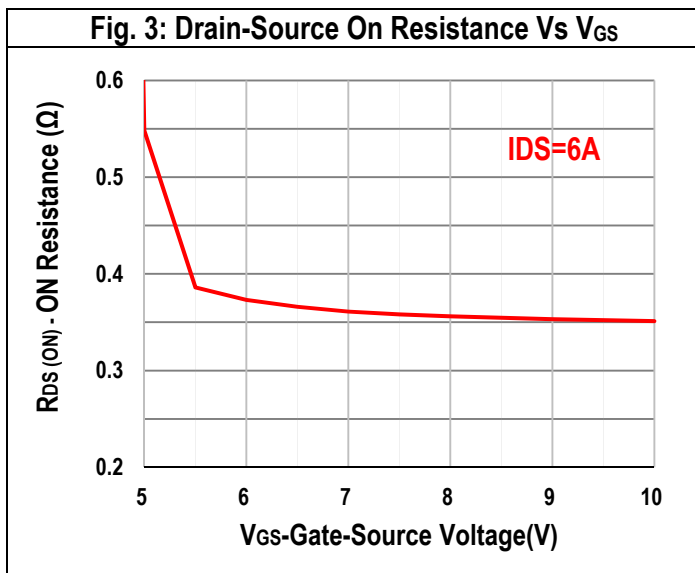
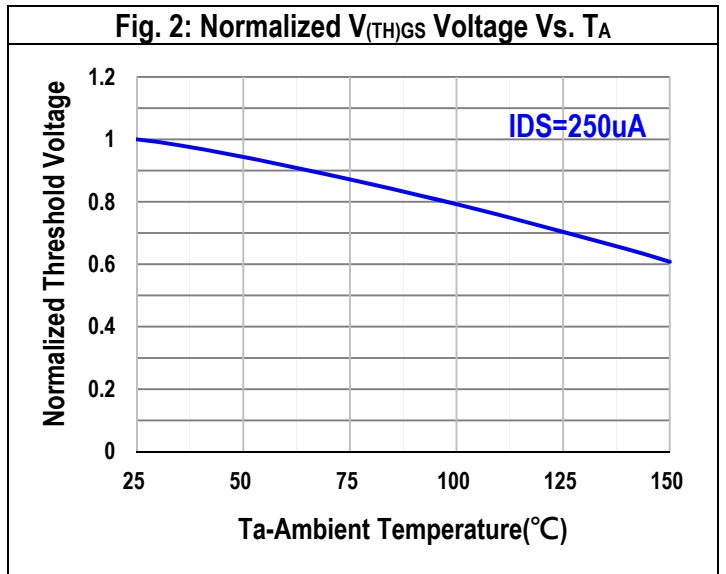
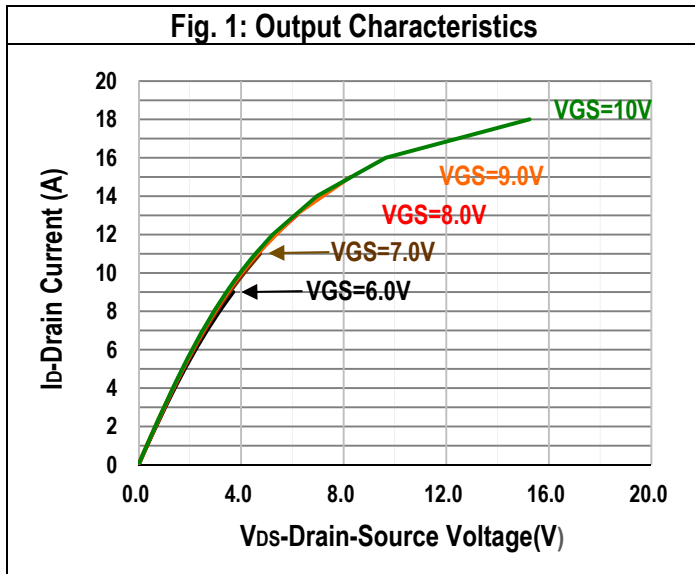
STATIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _{DS} =250μA	2.8	3.0	3.3	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _{DS} =4.0A	-	0.35	0.38	Ω
Gate Resistance	R _G	V _{GS} =0V, V _{DS} =0V, f=1MHz	-	12.1	-	Ω
Forward Transconductance	g _{fs}	V _{DS} =10V, I _{DS} =6.0A	-	7	-	S

DYNAMIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C _{iss}	V _{DD} =650V, V _{DS} =325V, V _{GS} =0V, F=500KHz	-	732	-	pF
Output Capacitance	C _{oss}	V _{DD} =650V, V _{DS} =325V, V _{GS} =0V, F=500KHz	-	23.3	-	pF
Reverse Transfer Capacitance	C _{rss}	V _{DD} =650V, V _{DS} =325V, V _{GS} =0V, F=500KHz	-	6	-	pF
Effective output capacitance-energy	C _{o(er)}	V _{DD} =400V, V _G =10V, energy related ^{Note 6}	-	81.3	-	pF
Effective output capacitance-time	C _{o(tr)}	V _{DD} =400V, V _G =10V, time related ^{Note 7}	-	303	-	pF
Turn-On Delay Time	T _{d(on)}	V _{DS} =400V, V _{GS} =10V, I _{DS} =6.0A, R _{GEN} =10Ω	-	14.4	-	nS
Rise Time	t _r	V _{DS} =400V, V _{GS} =10V, I _{DS} =6.0A, R _{GEN} =10Ω	-	23.9	-	nS
Turn-Off Delay Time	T _{d(off)}	V _{DS} =400V, V _{GS} =10V, I _{DS} =6.0A, R _{GEN} =10Ω	-	58.3	-	nS
Fall Time	t _f	V _{DS} =400V, V _{GS} =10V, I _{DS} =6.0A, R _{GEN} =10Ω	-	44.1	-	nS

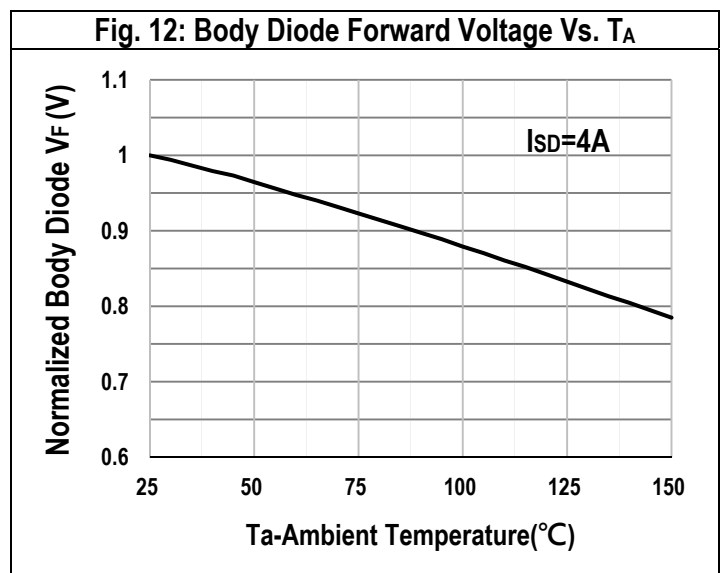
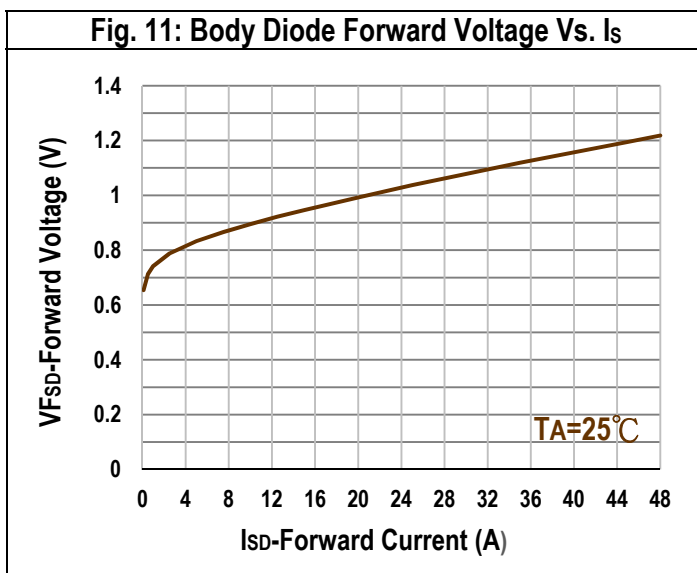
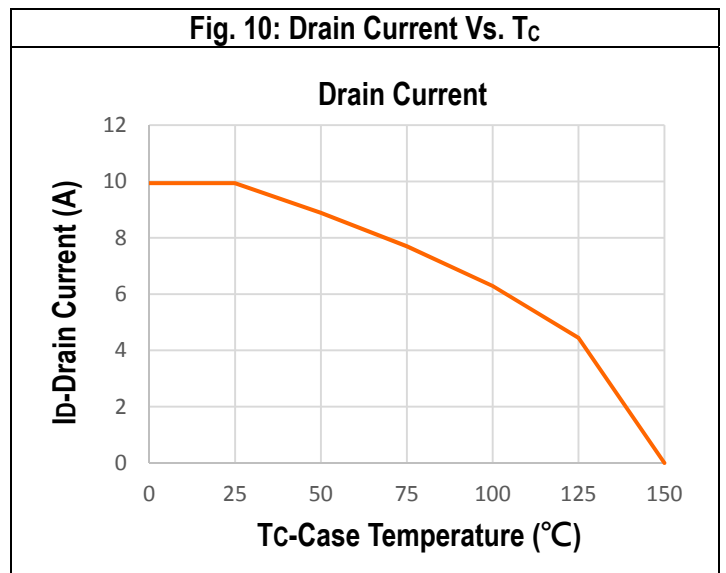
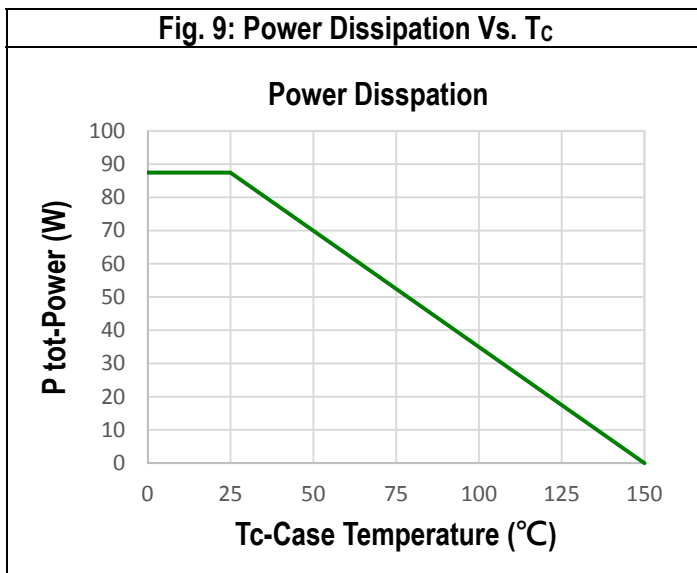
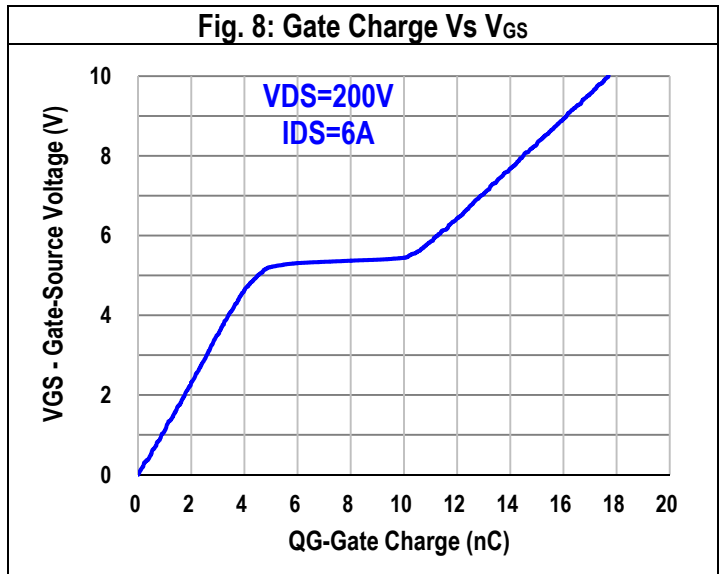
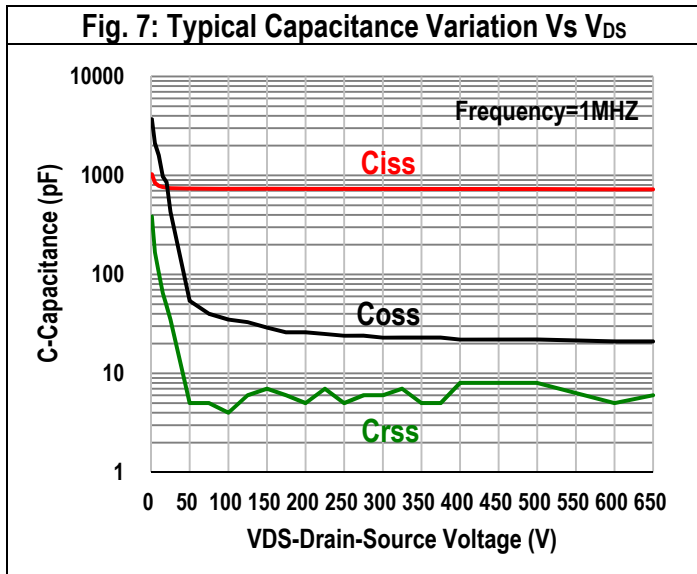
GATE CHARGE CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gate charge total	Q _{g 10V}	V _{DD} =200V, I _D =6.0A, V _{GS} =0 to 10V	-	17.6	-	nC
Gate to Source Gate Charge	Q _{gs}	V _{DD} =200V, I _D =6.0A, V _{GS} =0 to 10V	-	4.7	-	nC
Gate to Drain Charge	Q _{gd}	V _{DD} =200V, I _D =6.0A, V _{GS} =0 to 10V	-	5.7	-	nC
Gate plateau voltage	V _{plateau}	V _{DD} =200V, I _D =6.0A, V _{GS} =0 to 10V	-	5.4	-	V

BODY DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Diode continuous forward current	I _S	T _C =25°C	-	-	10	A
Diode pulsed forward current	I _{SM}	T _C =25°C	-	-	18	A
Diode forward Voltage	V _{SD}	T _C =25°C, V _{GS} =0V, I _S = 6A	-	0.84	1.0	V
Diode reverse Recovery Time	t _{rr}	V _{DD} =100V, I _{SD} =6.0A, T _C =25°C, di/dt=100A/μs	-	279	-	nS
Diode reverse Recovery Charge	Q _{rr}	V _{DD} =100V, I _{SD} =6.0A, T _C =25°C, di/dt=100A/μs	-	2008	-	nC
Diode peak reverse recovery current	I _{rm}	V _{DD} =100V, I _{SD} =6.0A, T _C =25°C, di/dt=100A/μs	-	14.3	-	A

4. Typical Operating Characteristics diagrams



4. Typical Operating Characteristics diagrams



4. Typical Operating Characteristics diagrams

Fig. 13: Safe Operation Area

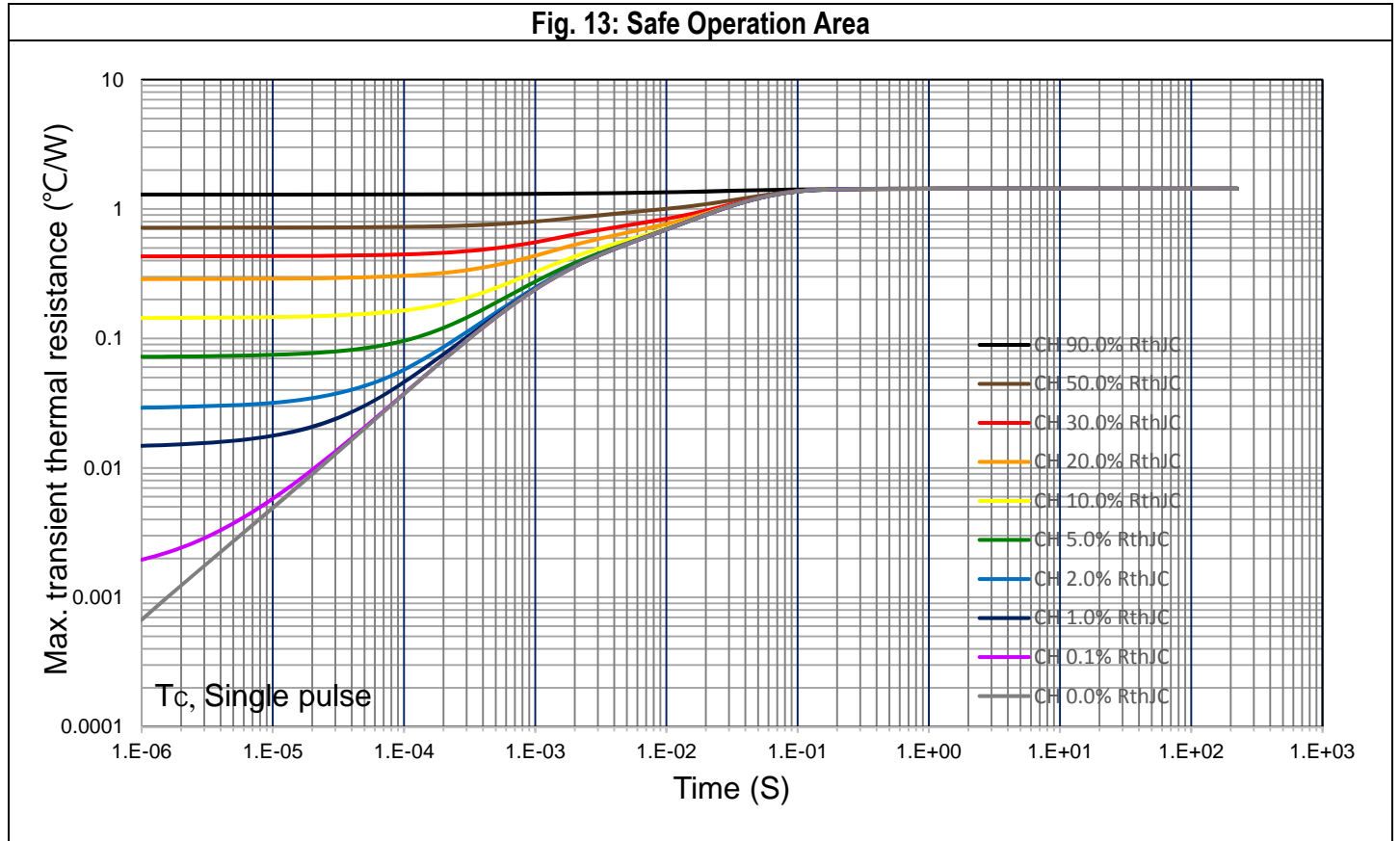
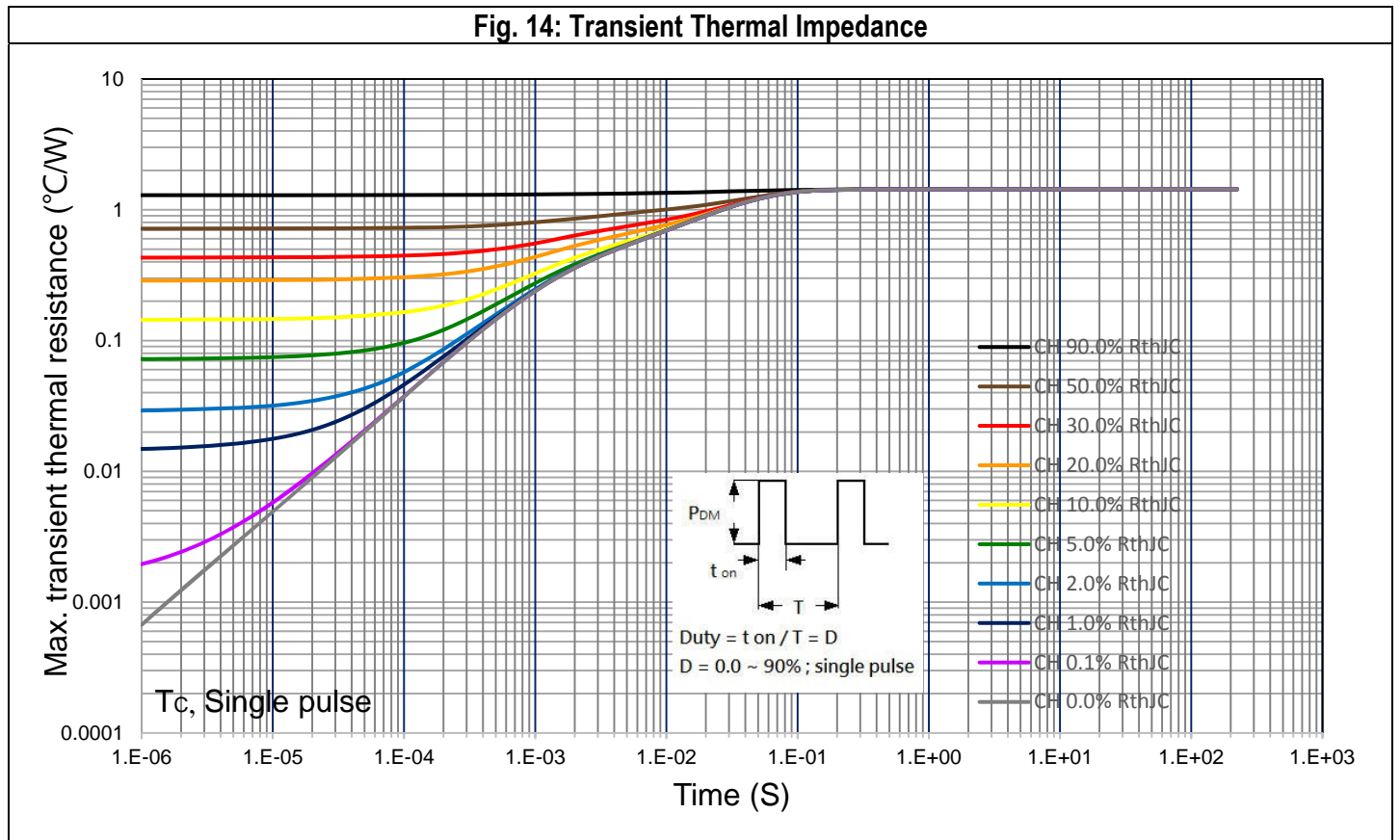


Fig. 14: Transient Thermal Impedance



5. Measurement Schematic

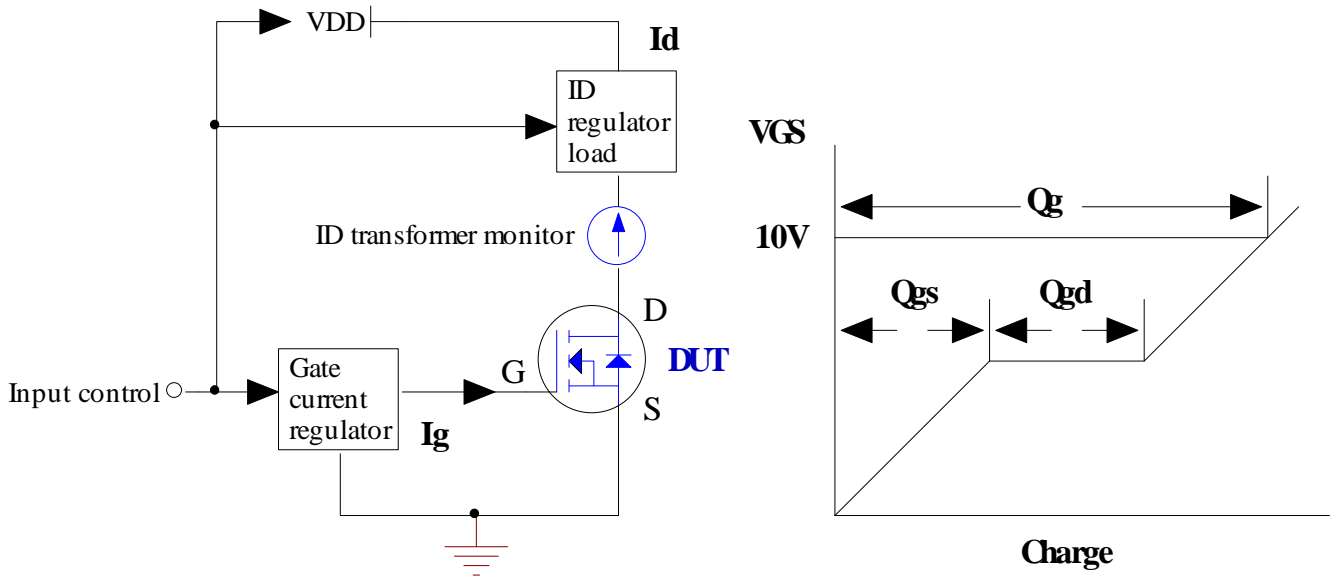


Diagram 5.1 Gate Charge Measurement Circuit and Waveforms

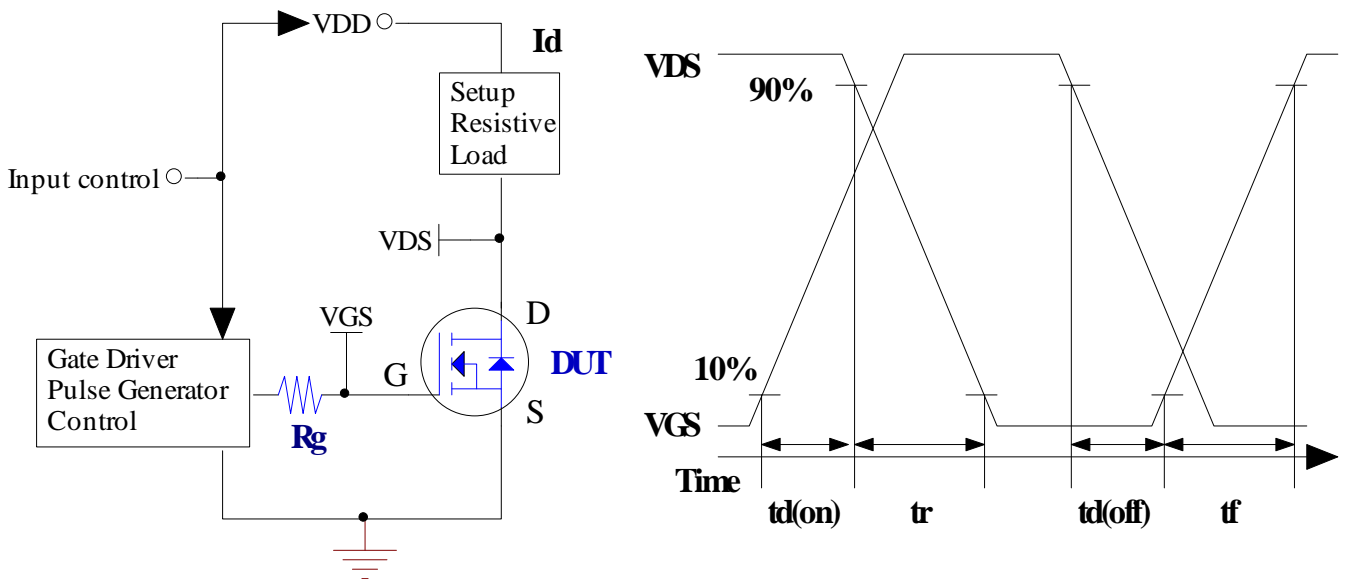


Diagram 5.2 Resistive Switching Measurement Circuit and Waveforms

5. Measurement Schematic

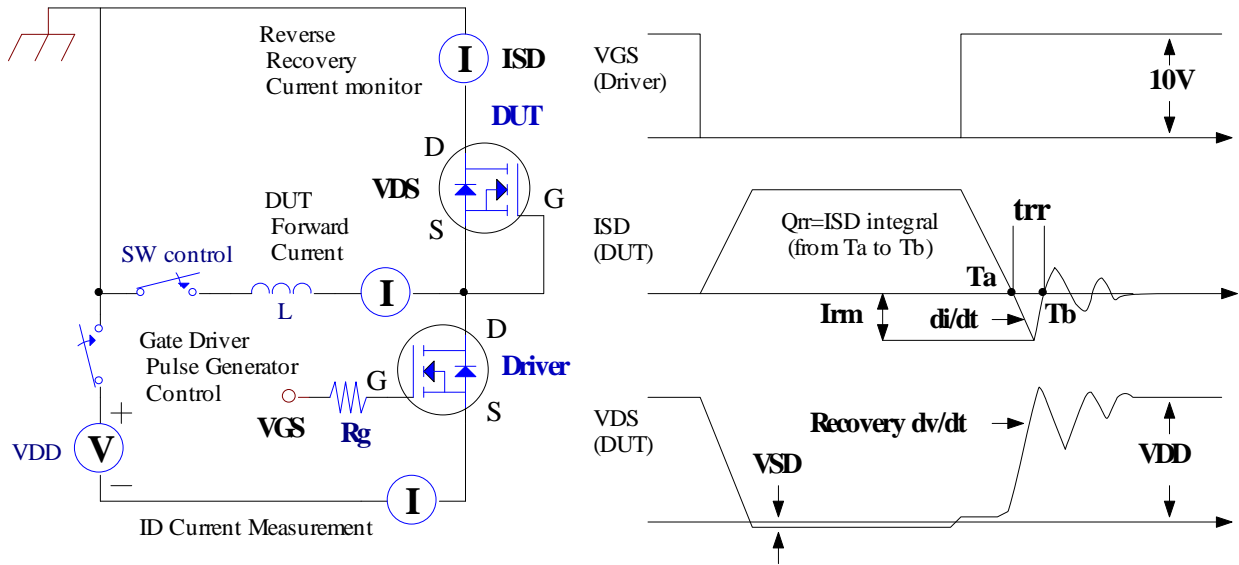


Diagram 5.3 Body Diode Recovery Characteristics Measurement Circuit and Waveforms

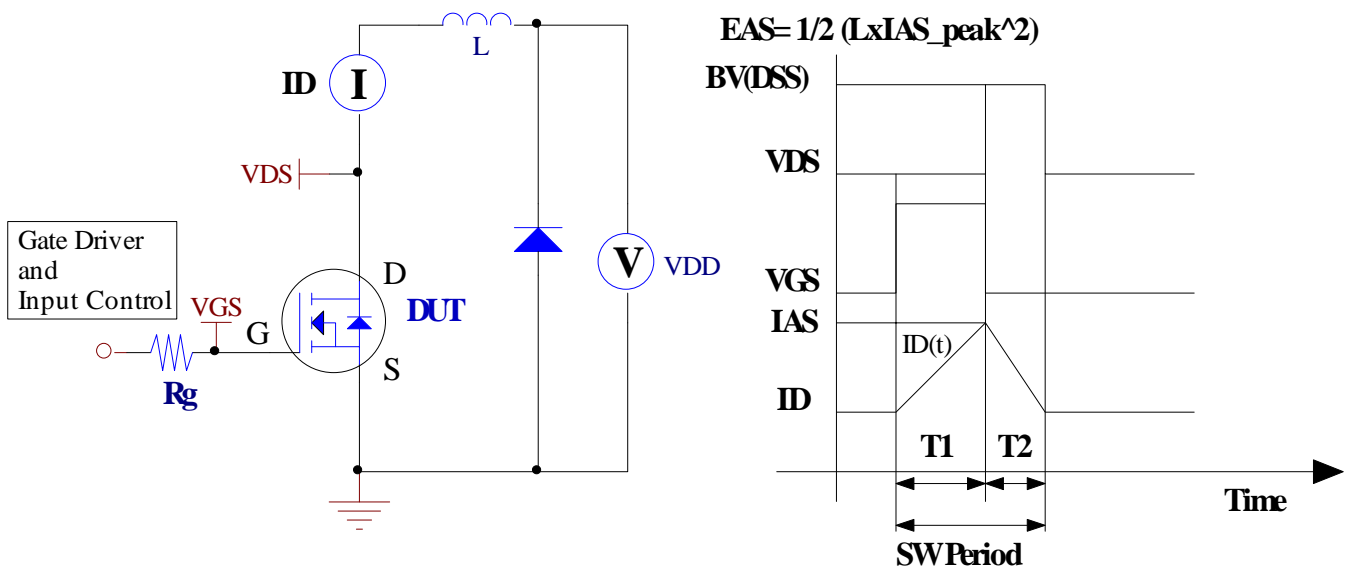
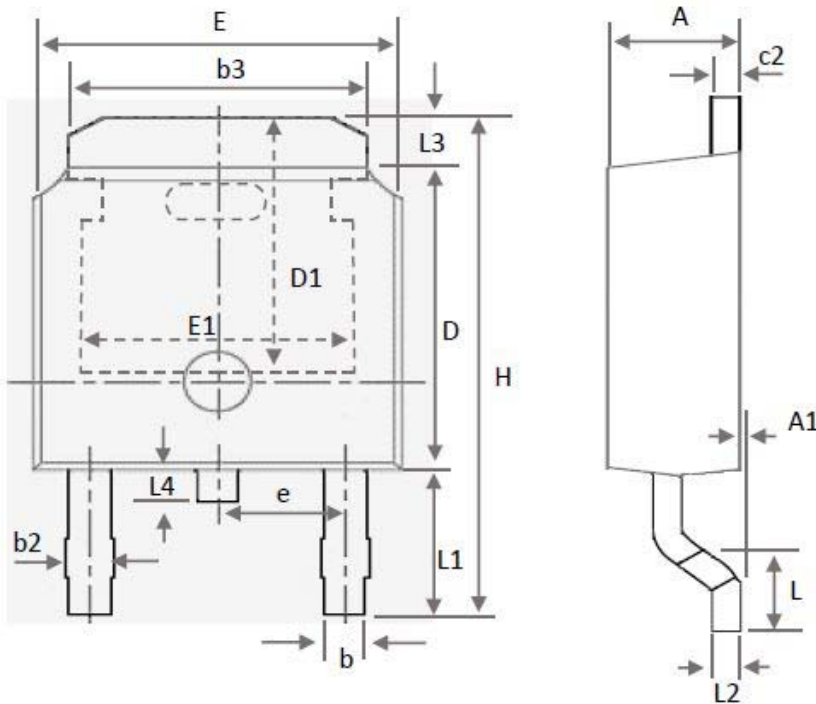


Diagram 5.4 Unclamped Inductive Switching Measurement Circuit and Waveforms

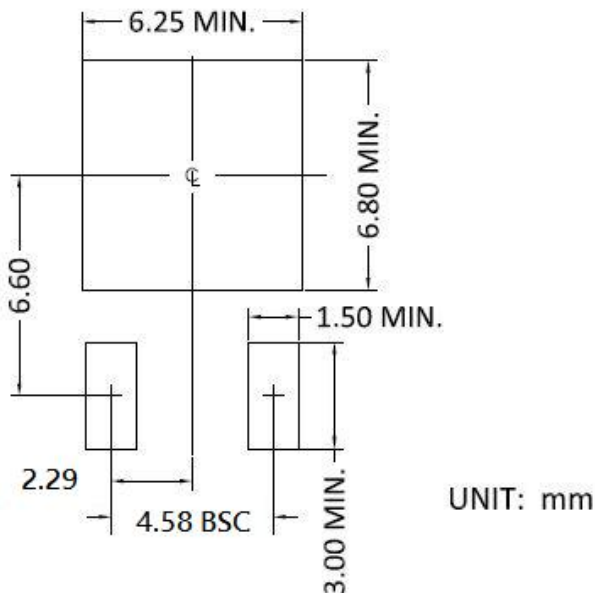
6. Package of Dimension

Package type: TO-252



Symbol	Min	Nor	Max
E	6.35	6.54	6.731
L	1.40	1.59	1.78
L1	2.743 Ref.		
L2	0.508 BSC		
L3	0.89	1.08	1.27
L4	0.60	0.81	1.01
D	5.97	6.10	6.223
H	9.40	9.91	10.41
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	4.95	5.21	5.46
e	2.286 BSC		
A	2.18	2.29	2.39
A1	0.00	0.07	0.13
c2	0.46	0.68	0.89
D1	5.21	-	-
E1	4.32	-	-

7. Land pattern (Footprint)



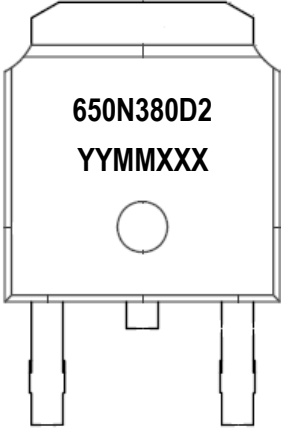
Note 1: Land pattern (Footprint) design is for reference only.

Note 2: Package body sizes exclude mold flash and burrs.

Note 3: Dimension is measured in gauge plane.

Note 4: Tolerance 0.1mm unless otherwise specified.

8. Marking Information

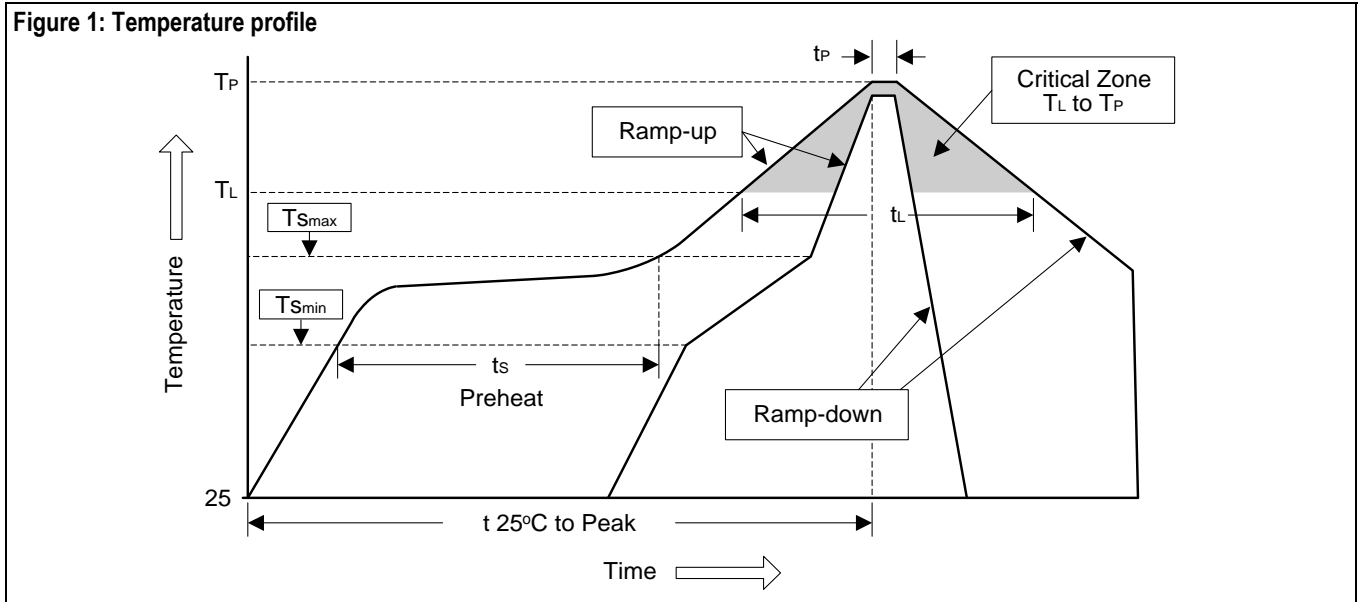
TO-252 (D)	Marking Rule
<p>Laser Marking</p>  <p>The diagram shows a TO-252 (D) MOSFET package. On the top surface, there is a laser marking consisting of two lines of text: '650N380D2' on the top line and 'YYMMXXX' on the bottom line. The package has three leads extending from the bottom.</p>	<p><u>Line 1</u> : Device 650N380D2</p> <p><u>Line 2</u> : Date Code YYMMXXX</p> <p>YY : Year Code MM : Month Code XXX : Serial Number</p>

9. Appendix

Appendix-A

Soldering Methods for Silicongear's Products (Just for SMD type of device)

1. Storage environment: Temperature=10°C to 35°C Humidity=65%±15%
2. Reflow soldering of surface-mount devices



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	<3°C/sec	<3°C/sec
Preheat		
- Temperature Min (T_{Smin})	100°C	150°C
- Temperature Max (T_{Smax})	150°C	200°C
- Time (min to max) (t_s)	60 to 120 sec	60 to 180 sec
T_{Smax} to T_L		
- Ramp-up Rate	<3°C/sec	<3°C/sec
Time maintained above:		
- Temperature (T_L)	183°C	217°C
- Time (t_L)	60 to 150 sec	60 to 150 sec
Peak Temperature (T_P)	240°C +0/-5°C	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10 to 30 sec	20 to 40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25°C to Peak Temperature	<6 minutes	<8 minutes

3. Flow (wave) soldering (solder dipping)

Products	Peak Temperature	Dipping Time
Pb devices.	245°C ±5°C	5sec ±1sec
Pb-Free devices.	260°C +0/-5°C	5sec ±1sec

9. Appendix**Appendix-B****Important Notice****© Silicongear Corporation**

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